REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add burn-in condition C to 4.2.a.1 and 4.3.2b.1. Device types 03 and 04 inactive for new design. Not available from an approved source. Editorial changes throughout.	90-07-03	W. Heckman
B	Add burn-in condition A to 4.2.a.1 and 4.3.2.b.1	91-11-14	M. Poelking
C	Add device types 05 and 06. Editorial changes throughout.	92-12-11	M. Poelking
D	Correct descriptive designator for case outline K. Update boilerplate to meet MIL-PRF-38535 requirements. Add vendor CAGE 0DKS7. - LTG	02-12-10	Thomas M. Hess
E	Correct section 1.3, supply voltage range and formula for DC output current and total DC V_{CC} current. Update boilerplate paragraphs to the current requirements in as specified in MIL-PRF-38535. - jak	10-01-20	Thomas M. Hess
F	Update boilerplate paragraphs to meet MIL-PRF-38535 requirements. Update supplier information. - MAA	17-06-19	Thomas M. Hess

REV																				
SHEET																				
REV	F	F	F																	
SHEET	15	16	17																	

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Tim H. Noh

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
87-12-02

REVISION LEVEL
F

MICROCIRCUIT, DIGITAL, HIGH PERFORMANCE CMOS 9-WIDE AND 10-WIDE BUS INTERFACE REGISTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88516**

SHEET 1 OF 17

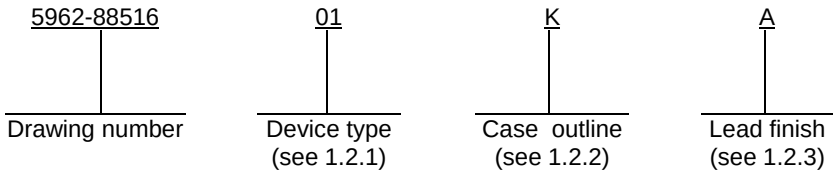
DSCC FORM 2233
APR 97

5962-E324-17

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	29C821	High performance CMOS 10-wide bus interface register
02	29C823	High performance CMOS 9-wide bus interface register
03	29C921	High performance CMOS 10-wide bus interface register (rotated die) 1/
04	29C921	High performance CMOS 9-wide bus interface register (rotated die) 1/
05	29C821A	High performance CMOS 10-wide bus interface register (edge-rate controlled outputs)
06	29C823A	High performance CMOS 9-wide bus interface register (edge-rate controlled outputs)

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat package
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
3	CQCC1-N28	28	Square leadless-chip-carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1/ Not available from an approved source of supply.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
DC input voltage range	
Devices 01-04	-0.5 V dc to V_{CC} + 0.5 V dc
Devices 05,06	-0.5 V dc to +6.0 V dc
DC output voltage range	
Devices 01-04	-0.5 V dc to V_{CC} + 0.5 V dc
Devices 05,06	-0.5 V dc to +6.0 V dc
DC output diode current: In to output	
All devices	+50 mA
DC output diode current: out of output	
All devices	-50 mA
DC input diode current: Into output	
All devices	+20 mA
DC input diode current: out of output	
All devices	-20 mA
DC output current per pin (I_{sink})	
Devices 01-04	+48 mA (2 x I_{OL})
Devices 05,06	+100 mA
DC output current per pin (I_{source})	
Devices 01-04	-30 mA (2 x I_{OH})
Devices 05,06	-100 mA
Total dc ground current	(n x I_{OL} + m x I_{CCT}) mA 1/
Total dc V_{CC} current	(n x I_{OH} + m x I_{CCT}) mA 1
Maximum power dissipation (P_D) 2/	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases L, K, and 3	See MIL-STD-1835
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc

1/ n = number of outputs, m = number of inputs.
2/ For T_A = +100°C to +125°C derate linearly at 10mW/°C.

2. APPLICABLE DOCUMENTS m

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -15.0 mA $V_{IN} = V_{IL}, V_{IH}$		1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V $V_{IN} = V_{IL}, V_{IH}$	I_{OL} = +24.0 Ma	1, 2, 3	01-04		0.5	V
			I_{OL} = +32.0 Ma		05,06		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 Ma		1, 2, 3	All		-1.2	V
Low level input current	I_{IL1}	V_{CC} = 5.5 V	V_{IN} = 0 V	1, 2, 3	01-04		-10	µA
					05,06		-5	µA
	I_{IL2}		V_{IN} = 0.4 V		01-04		5	µA
High level input current	I_{IH1}	V_{CC} = 5.5 V	V_{IN} = 2.7 V	1, 2, 3	01-04		5	µA
	I_{IH2}		V_{IN} = 5.5 V		01-04		10	µA
					05,06		5	µA
Off state current	I_{OZH}	V_{CC} = 5.5 V	V_{OUT} = 5.5 V	1, 2, 3	All		10	µA
	I_{OZL}		V_{OUT} = 0.0 V	1, 2, 3	All		-10	µA
Output short circuit current	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0 V 1/		1, 2, 3	All	-60		mA
Static supply current	I_{CCQ}	V_{CC} = 5.5 V, outputs open V_{IN} = 5.5 V or GND		1, 2, 3	01-04		160	µA
					05,06		1500	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Static supply current	I_{CCT}	V_{CC} = 5.5 V, Outputs open V_{IN} = 3.4 V	Data input	1, 2, 3	All		1.5	mA/bit
			$\overline{OE}$, CP		01,03, 05		3.0	
			$\overline{OE}$, $\overline{EN}$ CLR, CP		02,04,06		3.0	
Input capacitance	C_{IN}	See 4.3.1c		4	All		16	pF
Output capacitance	C_{OUT}	See 4.3.1c		4	All		20	pF
Functional testing		See 4.3.1d		7,8	All			
Propagation delay clock (CP) to Y_I	t_{PLH}	See figure 4 C_L = 50 pF R_1 = 500Ω R_2 = 500Ω		9,10,11	01-04		14	ns
				9, 10, 11	05,06		9.5	ns
Propagation delay clock (CP) to Y_I	t_{PHL}			9,10,11	01-04		14	ns
				9, 10, 11	05,06		9.5	ns
Propagation delay clear to Y_I	t_{PHL}			9,10,11	02, 04		15	ns
					06		10.5	ns
Propagation delay output enable (OE) to Y_I	t_{PZH}			9,10,11	01-04		14	ns
					05,06		9	ns
	t_{PZL}			9,10,11	01-04		14	ns
					05,06		13	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay output disable (OE) to Y_I	t_{PHZ}	See figure 4 $C_L = 50$ pF $R_1 = 500\Omega$ $R_2 = 500\Omega$	9,10,11	01-04		14	ns
				05,06		8.5	ns
	t_{PLZ}		9,10,11	01-04		14	ns
				05,06		8.5	ns
Data (D_I) to CP setup time	t_S		9,10,11	01-04	6		ns
				05,06	3		ns
Data (D_I) to CP hold time	t_H		9,10,11	01-04	3		ns
				05,06	2		ns
Enable (high to low) to CP setup	t_S		9,10,11	02, 04	6		ns
				06	4		ns
Enable (low to high) to CP setup	t_S		9,10,11	02, 04	6		ns
				06	4		ns
Enable hold time	t_H		9,10,11	02, 04	3		ns
				06	0		ns
Clear (low to high) to CP setup time	t_S		9,10,11	02, 04	6		ns
	t_{REC}			06	6		ns
Clock low pulse width	t_{PWL}		9,10,11	01-04	11		ns
				05,06	6		ns
Clock high pulse	t_{PWH}		9,10,11	01-04	11		ns
				05,06	6		ns
Clear pulse width	t_{PWL}		9,10,11	02, 04	11		ns
				06	6		ns

1/ Not more than one output shorted at a time. Duration should not exceed 100 miliseconds.

Device types	01 and 05	
Case outlines	K and L	3
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{OE}$	NC
2	D_0	$\overline{OE}$
3	D_1	D_0
4	D_2	D_1
5	D_3	D_2
6	D_4	D_3
7	D_5	D_4
8	D_6	NC
9	D_7	D_5
10	D_8	D_6
11	D_9	D_7
12	GND	D_8
13	CP	D_9
14	Y_9	GND
15	Y_8	NC
16	Y_7	CP
17	Y_6	Y_9
18	Y_5	Y_8
19	Y_4	Y_7
20	Y_3	Y_6
21	Y_2	Y_5
22	Y_1	NC
23	Y_0	Y_4
24	V_{CC}	Y_3
25	----	Y_2
26	----	Y_1
27	----	Y_0
28	----	V_{CC}

NC = No internal connection

s

FIGURE 1 Terminal connections.

Device types	02 and 06	
Case outlines	K and L	3
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{OE}$	NC
2	D_0	$\overline{OE}$
3	D_1	D_0
4	D_2	D_1
5	D_3	D_2
6	D_4	D_3
7	D_5	D_4
8	D_6	NC
9	D_7	D_5
10	D_8	D_6
11	$\overline{CLR}$	D_7
12	GND	D_8
13	CP	$\overline{CLR}$
14	$\overline{EN}$	GND
15	Y_8	NC
16	Y_7	CP
17	Y_6	$\overline{EN}$
18	Y_5	Y_8
19	Y_4	Y_7
20	Y_3	Y_6
21	Y_2	Y_5
22	Y_1	NC
23	Y_0	Y_4
24	V_{CC}	Y_3
25	----	Y_2
26	----	Y_1
27	----	Y_0
28	----	V_{CC}

NC = No internal connection.

FIGURE 1. Terminal connections – Continued.

Device types	03	04
Case outlines	L	L
Terminal number	Terminal symbol	Terminal symbol
1	Y_4	Y_4
2	Y_3	Y_3
3	Y_2	Y_2
4	Y_1	Y_1
5	Y_0	Y_0
6	V_{CC}	V_{CC}
7	$\overline{OE}$	$\overline{OE}$
8	D_0	D_0
9	D_1	D_1
10	D_2	D_2
11	D_3	D_3
12	D_4	D_4
13	D_5	D_5
14	D_6	D_6
15	D_7	D_7
16	D_8	$\overline{D_8}$
17	D_9	$\overline{CLR}$
18	GND	GND
19	CP	CP
20	Y_9	$\overline{EN}$
21	Y_8	Y_8
22	Y_7	Y_7
23	Y_6	Y_6
24	Y_5	Y_5

FIGURE 1. Terminal connections – Continued.

Device types 01, 03, and 05

Inputs			Internal	Outputs	Function
$\overline{OE}$	D_i	CP	$\overline{Q}_i$	Y_i	
H H	L H	↑ ↑	H L	Z Z	Hi-Z
L L	L H	↑ ↑	H L	L H	Load

Device types 02, 04, and 06

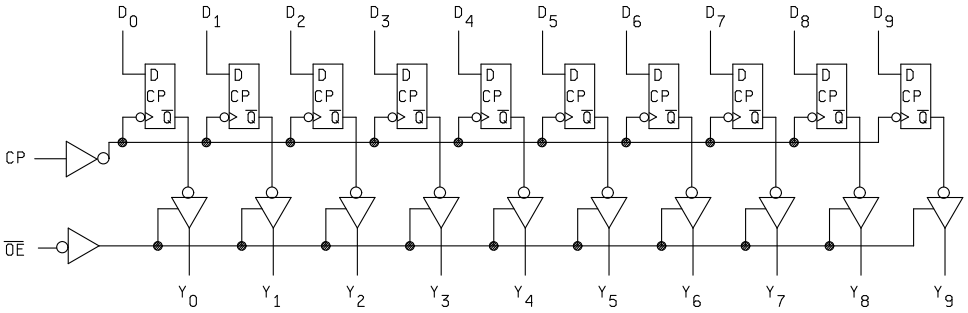
Inputs					Internal	Outputs	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q}_i$	Y_i	
H H	H H	L L	L H	↑ ↑	H L	Z Z	Hi-Z
H L	L L	X X	X X	X X	H H	Z L	Clear
H L	H H	H H	X X	X X	NC NC	Z NC	Hold
H H L L	H H H H	L L L L	L H L H	↑ ↑ ↑ ↑	H L H L	Z Z L H	Load

H = High
L = Low
X = Irrelevant

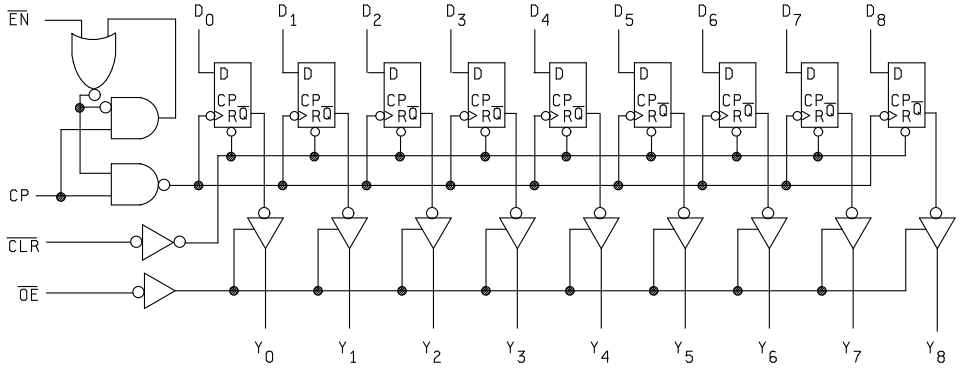
NC = No change
↑ = Low-to-high transition
Z = High impedance

FIGURE 2. Truth tables.

Device types 01, 03, and 05



Device types 02 and 04



Device type 06

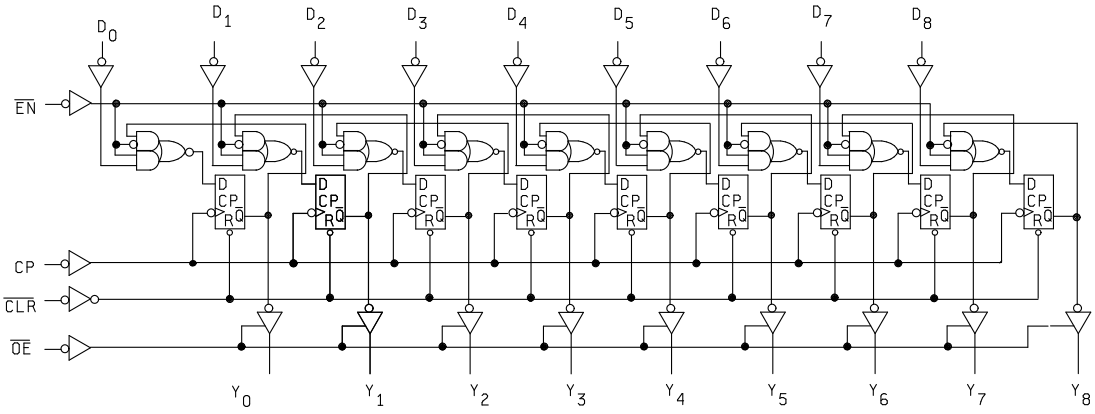
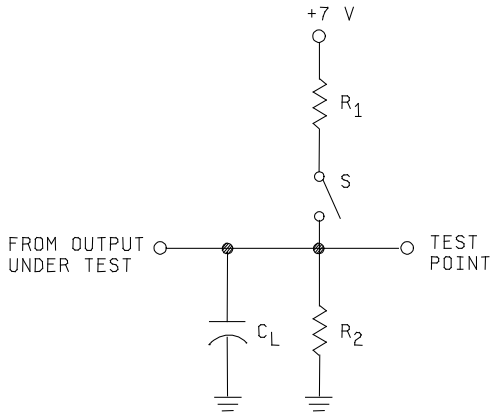


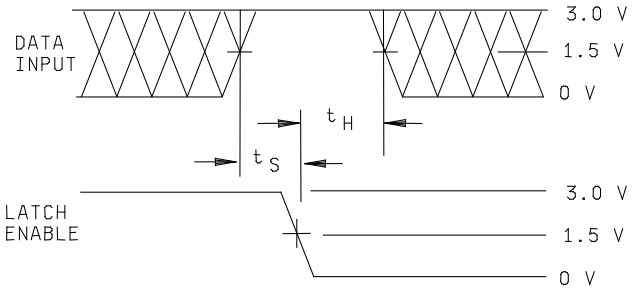
FIGURE 3. Logic diagrams.



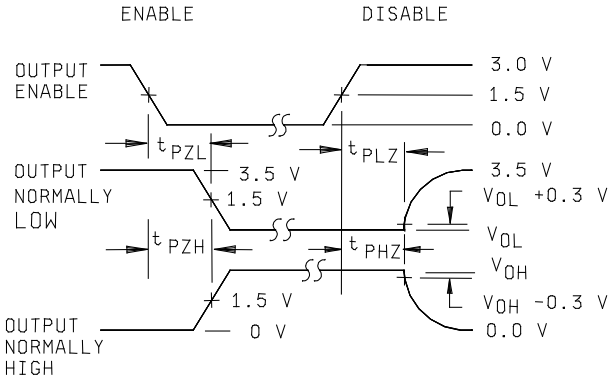
Load circuit for three-state outputs

Parameter	S Position
t_{PLH}	Open
t_{PHL}	Open
t_{PHZ}	Open
t_{PZH}	Open
t_{PLZ}	Closed
t_{PZL}	Closed

Setup and hold times



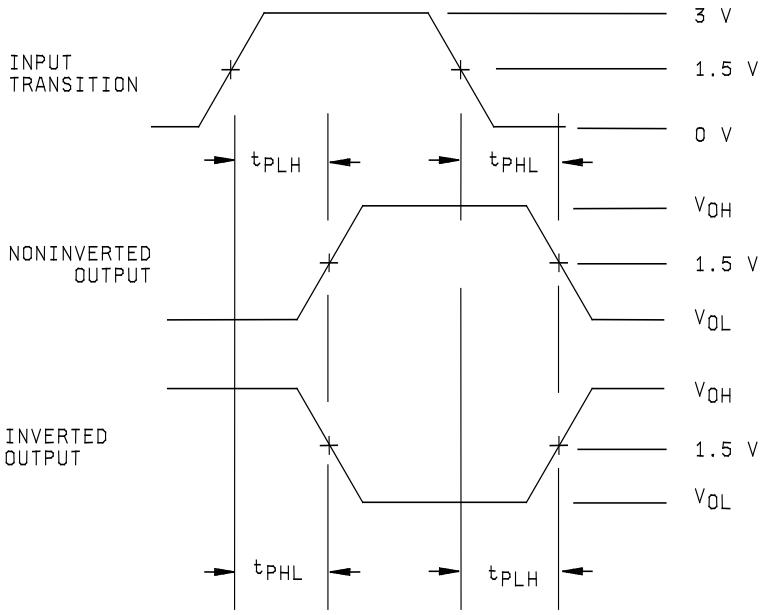
Enable and disable times



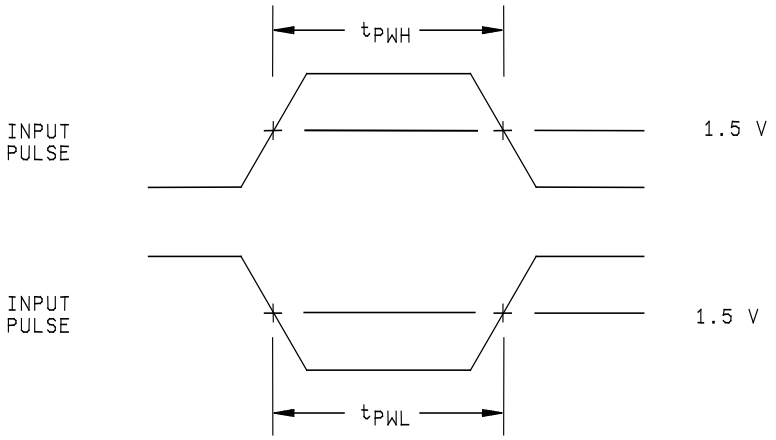
NOTES:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

FIGURE 4. Test circuit and switching waveforms.

Propagation delay



Pulse width



NOTE: Pulse generator for all pulses rate ≤ 1.0 MHz; Z_o = 500Ω;
t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

FIGURE 4. Test circuit and switching waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth tables.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-06-19

Approved sources of supply for SMD 5962-88516 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Generic part number 2/
5962-88516013A	0DKS7	GEM19401Q3A	29C821
5962-88516013C	0DKS7	GEM19401Q3C	29C821
5962-8851601KA	0DKS7	GEM19401QKA	29C821
5962-8851601KC	0DKS7	GEM19401QKC	29C821
5962-8851601LA	0DKS7	GEM19401QLA	29C821
5962-8851601LC	0DKS7	GEM19401QLC	29C821
5962-88516023A	0DKS7	GEM18902Q3A	29C823
5962-88516023C	0DKS7	GEM18902Q3C	29C823
5962-8851602KA	0DKS7	GEM18902QKA	29C823
5962-8851602KC	0DKS7	GEM18902QKC	29C823
5962-8851602LA	0DKS7	GEM18902QLA	29C823
5962-8851602LC	0DKS7	GEM18902QLC	29C823
5962-8851603LX	3/		29C921
5962-8851604LX	3/		29C923
5962-8851605LX	3/		29C821
5962-8851605KX	3/		29C821
5962-88516053X	3/		29C821
5962-8851606LX	3/		29C823
5962-8851606KX	3/		29C823
5962-88516063X	3/		29C823

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0DKS7	SRI International 201 Washington Road Princeton, NJ 08540-6449