National Semiconductor

CD4076BM/CD4076BC TRI-STATE® Quad D Flip-Flop

General Description

The CD4076BM/CD4076BC TRI-STATE quad D flip-flop is a monlithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. The four D type flip-flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disables allow the flip flops to remain in their present state without disrupting the clock. If either of the two input disables is taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

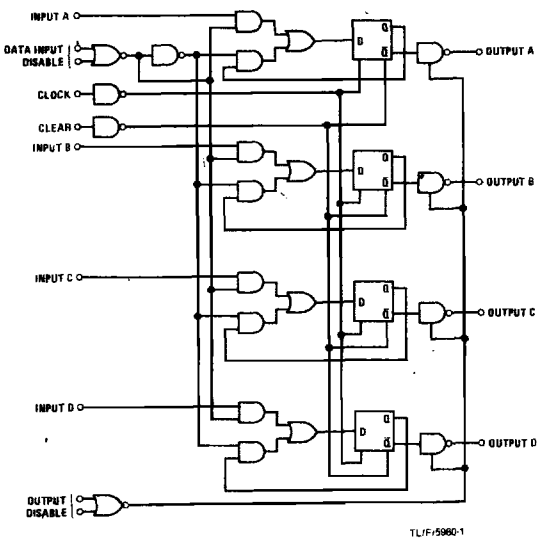
Clearing is enabled by taking the clear input to a logic "1" level. Clocking occurs on the positive-going transition.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

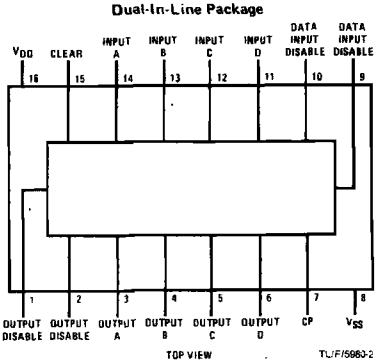
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- High impedance TRI-STATE outputs
- Inputs can be disabled without gating the clock
- Equivalent to MM54C173/MM74C173

Logic and Connection Diagrams



Dual-In-Line Package



Order Number CD4076BMJ or CD4076BCJ
See NS Package J16A

Order Number CD4076BMN or CD4076BCN
See NS Package N16E

Truth Table

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4076BM	−55°C to +125°C
CD4076BC	−40°C to +85°C

DC Electrical Characteristics CD4076BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	Output Current in High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4076BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA

DC Electrical Characteristics (Cont'd.) CD4076BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	Output Current in High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, $R_L = 200k$, Input $t_r = t_f = 20ns$, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Output	V_{DD} = 5V		220	400	ns
		V_{DD} = 10V		80	200	ns
		V_{DD} = 15V		65	160	ns
t_{PHL}	Propagation Delay Time From Clear to Output	V_{DD} = 5V		240	490	ns
		V_{DD} = 10V		90	180	ns
		V_{DD} = 15V		70	145	ns
t_{SU}	Minimum Input Data Set-Up Time	V_{DD} = 5V		40	80	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
t_H	Minimum Input Data Hold Time	V_{DD} = 5V		−40	0	ns
		V_{DD} = 10V		−12	0	ns
		V_{DD} = 15V		−10	0	ns
t_{SU}	Minimum Input Disable Set-Up Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		35	70	ns
		V_{DD} = 15V		28	55	ns
t_H	Minimum Input Disable Hold Time	V_{DD} = 5V		−75	0	ns
		V_{DD} = 10V		−30	0	ns
		V_{DD} = 15V		−25	0	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time From Output Disable to High Impedance State	V_{DD} = 5V, R_L = 1.0k		170	340	ns
		V_{DD} = 10V, R_L 1.0k		70	140	ns
		V_{DD} = 15V, R_L 1.0k		56	115	ns
	Propagation Delay From Output Disable to Logical "1" Level or Logical "0" Level (From High Impedance State)	V_{DD} = 5V, R_L = 1.0k		170	340	ns
		V_{DD} = 10V, R_L = 1.0k		70	140	ns
		V_{DD} = 15V, R_L = 1.0k		56	115	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	3.0	4.0		MHz
		V_{DD} = 10V	7.0	12.0		MHz
		V_{DD} = 15V	8.75	15.0		MHz
t_{WH}	Minimum Clear Pulse Width	V_{DD} = 5V		150		ns
		V_{DD} = 10V		70		ns
		V_{DD} = 15V		56		ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	10			μs
		V_{DD} = 10V	5			μs
		V_{DD} = 15V	2			μs
C_{IN}	Average Input Capacitance	Data Inputs (A, B, C, D)		3	7.5	pF
		Other Inputs		6	15	pF
C_{PD}	Power Dissipation Capacity	All Four Flip-Flops, (Note 4)		100		pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output			15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

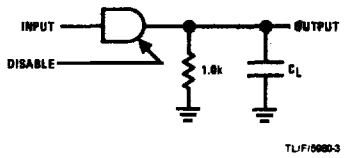
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

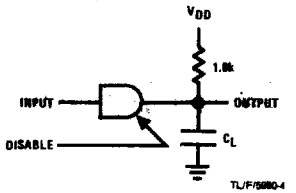
AC Test Circuits and Switching Time Waveforms

t_{PHZ} and t_{PZH}



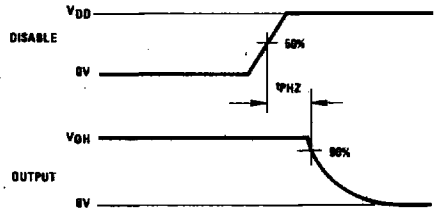
TL/F/5080-3

t_{PLZ} and t_{PZL}



TL/F/5080-4

t_{PHZ}



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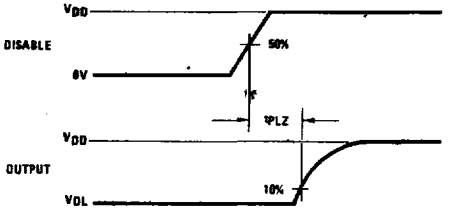
t_{PLZ}



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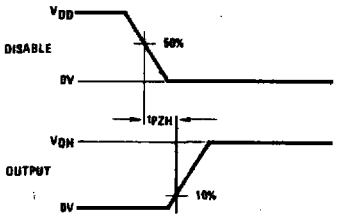
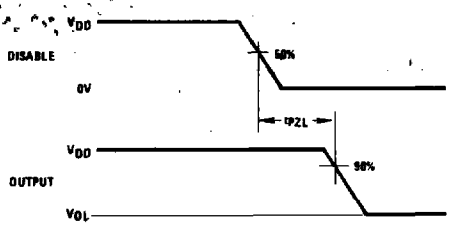
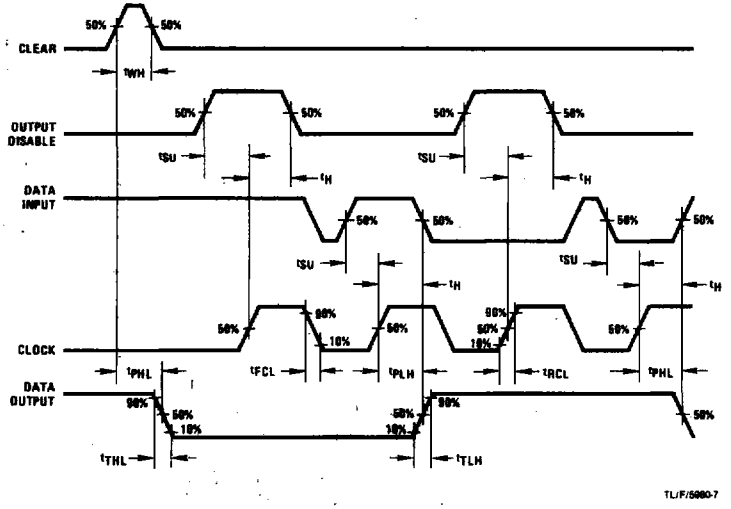
t_{PZH}



t_{PZL}





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