

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Bus Hold feature holds last active state during 3-state operation
- Industry standard pinouts
- 10 μ A I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V – 3.6V V_{CC} supply operation
- ± 24 mA balanced output drive
- Meets or exceeds JEDEC Standard 36 specifications
- $t_{PD} = 4.6$ ns
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- Operating temperature range:
 –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
 Human body model > 2000V
 Machine model > 200V
- Packages available:
 56-pin TSSOP
 56-pin SSOP

DESCRIPTION

The LCX16H501 is an 18-bit registered bus transceiver with three-state outputs that are ideal for driving address and data buses. These high-speed, low-power registered transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. The 3.3V LCXPlus family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end advanced workstation applications. 5V tolerant inputs and outputs allow this LCXPlus product to be used in mixed 5V and 3.3V applications. Bus Hold circuitry on the data inputs to retain the last active state during 3-state operation, eliminating the need for external pull-up resistors. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, of this product is designed not to load an active bus when V_{CC} is removed.

Figure 1. Functional Block Diagram

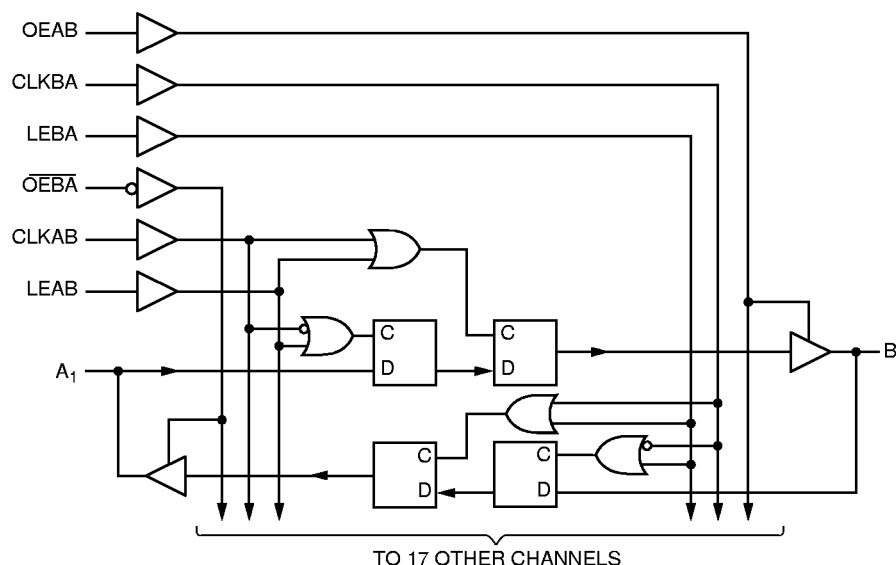


Figure 2. Pin Configuration
(All Pins Top View)

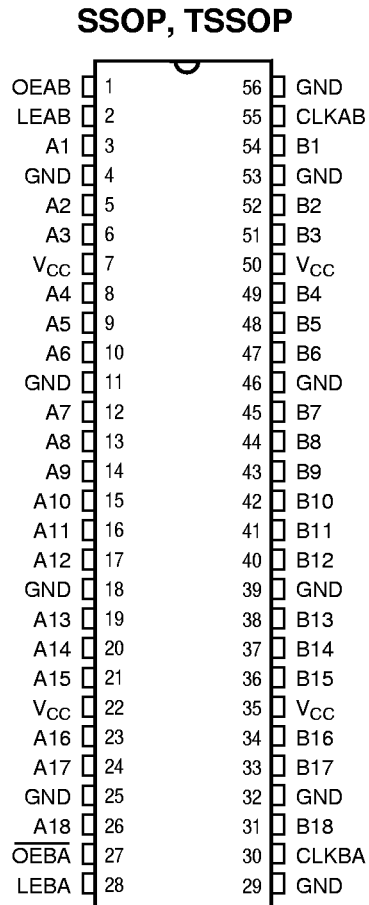


Table 1. Pin Description

Name	Description
OEAB	A-to-B Output Enable Input
\overline{OEBA}	B-to-A Output Enable Input (Active Low)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A _x	A-to-B Data Inputs or B-to-A 3-State Outputs
B _x	B-to-A Data Inputs or A-to-B 3-State Outputs

3

Table 2. Function Table⁽¹⁾

Inputs				Outputs
OEAB	LEAB	CLKAB	A _x	B _x
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B ⁽²⁾
H	L	L	X	B ⁽³⁾

Notes:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.

Table 3. Capacitance

Symbol	Pins	Typ	Unit	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz$
$C_{I/O}$	I/O Capacitance	8.0	pF	$V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz$
C_{PD}	Power Dissipation Capacitance	25	pF	$V_{CC} = 3.3V, V_{IN} = 0$ or V_{CC} $f = 10MHz$

Note: Capacitance is characterized but not production tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 7.0V
DC Output Voltage V_{OUT}	
Outputs HIGH-Z	-0.5V to 7.0V
Outputs Active	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_{IN}	-0.5V to 7.0V
DC Input Diode Current with $V_{IN} < 0$	-50mA
DC Output Diode Current	
$V_O < 0$	-50mA
$V_O > V_{CC}$	50mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	$\pm 50mA$
DC Supply Current per Supply Pin	$\pm 100mA$
DC Ground Current per Ground Pin	$\pm 100mA$
T_{STG} Storage Temperature	-65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage, Operating	2.0	3.6	V
	Supply Voltage, Data Retention Only	1.5	3.6	
V_{IN}	Input Voltage	0	5.5	V
V_{OUT}	Output Voltage in Active State	0	V_{CC}	V
	Output Voltage in "OFF" State	0	5.5	
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0 - 3.6V$	± 24	mA
		$V_{CC} = 2.7V$	± 12	
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
T_A	Operating Free Air Temperature	-40	85	°C

Table 6. DC Electrical Characteristics Over Operating RangeIndustrial Temperature Range, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.7\text{V}$, $I_{OH} = -100\mu\text{A}$ $V_{CC} = 2.7\text{V}$, $I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}$, $I_{OH} = -18\text{mA}$ $V_{CC} = 3.0\text{V}$, $I_{OH} = -24\text{mA}$	$V_{CC} - 0.2$ 2.2 2.4 2.2	— — — —	— — — —	V
V_{OL}	Output LOW Voltage	$V_{CC} = 2.7\text{V}$, $I_{OL} = 100\mu\text{A}$ $V_{CC} = 2.7\text{V}$, $I_{OL} = 12\text{mA}$ $V_{CC} = 3.0\text{V}$, $I_{OL} = 16\text{mA}$ $V_{CC} = 3.0\text{V}$, $I_{OL} = 24\text{mA}$	— — — —	— — — —	0.2 0.4 0.4 0.5	V
ΔV_T	Input Hysteresis ⁽³⁾	$V_{TLH} - V_{THL}$ for All Inputs	—	150	—	mV
I_I	Input Leakage Current	$V_I = 0\text{V}$, $V_I = 5.5\text{V}$, $V_{CC} = 3.6\text{V}$	—	—	± 1.0	μA
I_{OZ}	High-Z I/O Leakage ⁽³⁾	$V_O = 0\text{V}$, $V_O = 5.5\text{V}$, $V_I = V_{IH}$ or V_{IL} , $V_{CC} = 3.6\text{V}$	—	—	1.0	μA
I_{OS}	Short Circuit Current ^(3,4)	$V_{CC} = 3.6\text{V}$, $V_O = \text{GND}$	-60	—	-200	mA
I_{OFF}	Power Off Leakage	$V_{CC} = 0\text{V}$, V_I or $V_O = 5.5\text{V}$	—	—	10	μA
I_{BHH}	Input Current Input HIGH or LOW Bus Hold Inputs ^(3,5)	$V_{CC} = 3.6\text{V}$ $V_{IN} = 0\text{V}$ or $V_{IN} = V_{CC}$ $V_{CC} = 3.6\text{V}$, $0.8 \leq V_{IN} \leq 2.0\text{V}$	—	—	50 500 ⁽⁶⁾	μA μA
I_{BHH}	Bus Hold Sustaining Current	$V_{CC} = 3.3\text{V}$ $V_{IN} = 2.0\text{V}$	-75	—	—	μA
I_{BHL}	Bus Hold Inputs	$V_{IN} = 0.8\text{V}$	75	—	—	μA
V_{IK}	Input Clamp Voltage	$V_{CC} = 2.7$, $I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V

Notes:

1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values are at $V_{CC} = 3.3\text{V}$ and $T_A = 25^\circ\text{C}$
3. These parameters are guaranteed by characterization, but not production tested.
4. Not more than one output should be tested at one time. Duration of test should not exceed one second.
5. Pins with Bus Hold are identified in the Pin Description.
6. An external driver must provide at least $|I_{BH}|$ during transition to guarantee that the Bus Hold input will change state.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ ⁽²⁾	Max	Unit	
I_{CC}	Quiescent Power Supply Current	$V_{CC} = 3.6V$, Freq = 0 $V_{IN} = GND$ or V_{CC}	0.1	10	μA	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = 3.6V$, $V_{IN} = V_{CC} - 0.6V^{(3)}$	Control Inputs	2.0	30	μA
			Bus Hold Inputs	—	500	
I_{CCD}	Supply Current per Input per MHz ⁽⁴⁾	$V_{CC} = 3.6V$, Outputs Open One Bit Toggling @ 50% Duty Cycle OEAB = $\overline{OEBA} = V_{CC}$ LEAB = GND	$V_{IN} = V_{CC}$ $V_{IN} = GND$	100	130	$\mu A/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = 3.6V$, Outputs Open One Bit Toggling @ 50% Duty Cycle $f_{CP} = 10MHz$ (CLKAB) OEAB = $\overline{OEBA} = V_{CC}$ LEAB = GND $f_I = 5MHz$	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	0.5 ⁽⁵⁾	0.8 ⁽⁵⁾	mA
		$V_{CC} = 3.6V$, Outputs Open Eighteen Bits Toggling @ 50% Duty Cycle $f_{CP} = 10MHz$ (CLKAB) OEAB = $\overline{OEBA} = V_{CC}$ LEAB = GND $f_I = 2.5MHz$	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	3.4 ⁽⁵⁾	9.7 ⁽⁵⁾	mA

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
- Typical values are at $V_{CC} = 3.3V$, 25°C ambient.
- Per TTL driven input. All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in total power supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} f N_O$
 I_{CCQ} = Quiescent Current (I_{CCL} , I_{CCH} , and I_{CCZ}).
 ΔI_{CC} = Power Supply Current for a TTL-High Input ($V_{IN} = V_{CC} - 0.6V$).
 D_H = Duty Cycle for TTL High Inputs.
 N_T = Number of TTL High Inputs.
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
 f = Average Switching Frequency per Output.
 N_O = Number of Outputs Switching.

Table 8. Dynamic Switching Characteristics⁽¹⁾

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ C$	
				Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Note:

- Characterized but not production tested.

Table 9. Switching Characteristics Over Operating Range

Industrial Temperature Range, T_A = -40°C to 85°C

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description ⁽¹⁾	LCXH16501				LCXH16501C		Unit	
		V _{CC} = 3.3 ±0.3V		V _{CC} = 2.7V ⁽²⁾		V _{CC} = 3.3 ±0.3V			
		Min	Max	Min	Max	Min	Max		
f _{MAX}	CLKAB or CLKBA Frequency ⁽²⁾	170	—	—	—	170	—	MHz	
t _{PHL} t _{PLH}	Propagation Delay Ax to Bx or Bx to Ax	1.5	6.0	1.5	7.0	1.5	4.6	ns	
t _{PHL} t _{PLH}	Propagation Delay LEBA to Ax, LEAB to Bx	1.5	7.0	1.5	8.0	1.5	5.3	ns	
t _{PHL} t _{PLH}	Propagation Delay CLKBA to Ax, CLKAB to Bx	1.5	6.7	1.5	8.0	1.5	5.3	ns	
t _{PZH} t _{PZL}	Output Enable Time OEBA to Ax, OEAB to Bx	1.5	7.2	1.5	8.2	1.5	5.6	ns	
t _{PHZ} t _{PLZ}	Output Disable Time ⁽²⁾ OEBA to Ax, OEAB to Bx	1.5	7.0	1.5	8.0	1.5	5.2	ns	
t _{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA	2.5	—	3.0	—	3.0	—	ns	
t _H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA	0	—	0	—	0	—	ns	
t _{SU}	Setup Time HIGH or Low Ax to LEAB Bx to LEBA	Clock LOW	2.5	—	2.5	—	1.5	—	ns
		Clock HIGH	2.5	—	2.5	—	2.0	—	ns
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	1.5	—	1.5	—	1.5	—	ns	
t _W	Pulse Width ⁽²⁾	3.0	—	3.0	—	3.0	—	ns	
t _{SK(O)}	Output Skew ⁽³⁾	—	0.5	—	0.5	—	0.5	ns	

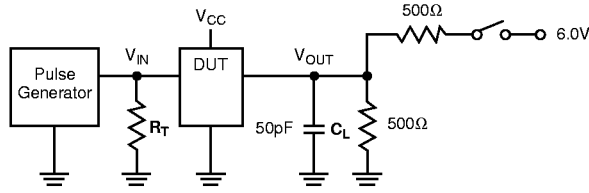
Notes:

1. See test circuit and waveforms. Minimum Limits are guaranteed but not tested on Propagation Delays.
2. Guaranteed by characterization.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by characterization but not production tested.

3

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit



SWITCH POSITION	
Test	Switch
Open Drain	
Disable LOW	6V
Enable LOW	
Disable HIGH	GND
Enable HIGH	
All Other Inputs	Open

DEFINITIONS:
 C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Figure 4. Setup, Hold, and Release Timing

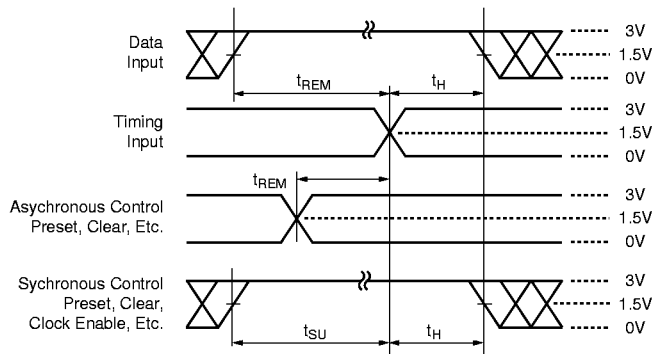


Figure 6. Pulse Width

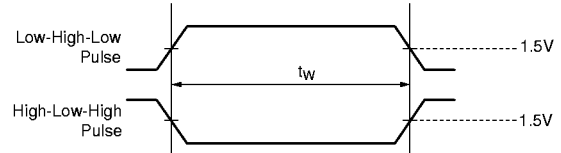


Figure 5. Enable and Disable Timing

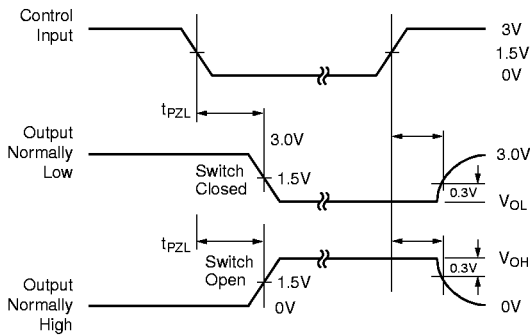
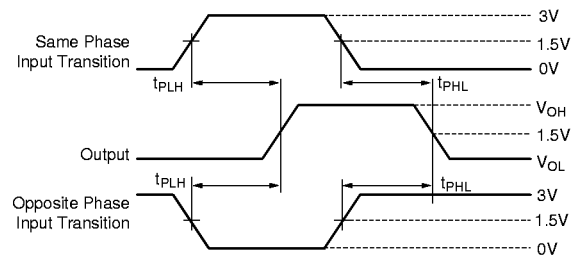


Figure 7. Propagation Delay

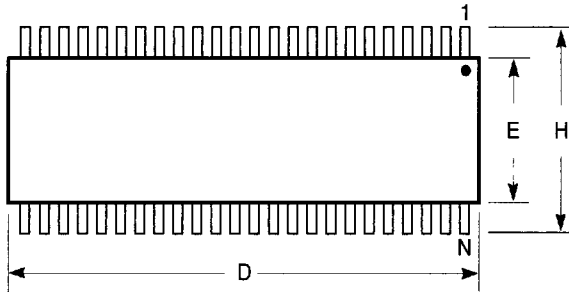


Notes:

1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz;
 $Z_{OUT} \leq 50\Omega$; $t_F, t_R \leq 2.5ns$.

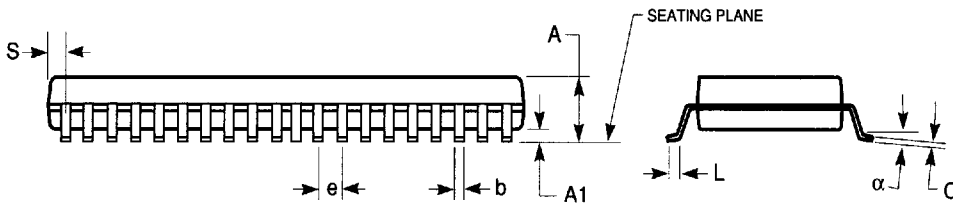
300-MIL SSOP - Package Code PV

**Shrink Small Outline Package
Plastic Small Outline Gull-Wing**



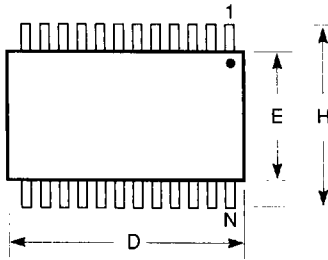
Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.



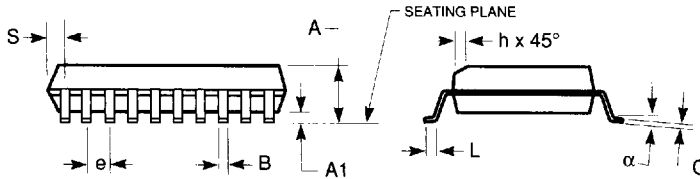
JEDEC#	MO-118AA			MO-118AB		
DWG#	PSS-48B			PSS-56B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.095	0.102	0.110	0.095	0.102	0.110
A1	0.008	0.012	0.016	0.008	0.012	0.016
b	0.008	0.010	0.0135	0.008	0.010	0.0135
C	0.005	0.008	0.010	0.005	0.008	0.010
D	0.620	0.625	0.630	0.720	0.725	0.730
E	0.291	0.295	0.299	0.291	0.295	0.299
e	0.025 BSC			0.025 BSC		
H	0.395	0.410	0.420	0.395	0.410	0.420
L	0.020	0.030	0.040	0.020	0.030	0.040
N	48			56		
α	0°	5°	8°	0°	5°	8°
S	0.022	0.025	0.028	0.022	0.025	0.028

170-MIL TSSOP - Package Code PA
Thin Shrink Small Outline Package
Plastic Small Outline Gull-Wing



Notes:

1. Refer to applicable symbol list.
2. N is the number of lead positions.
3. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
4. Lead coplanarity is 0.004in. maximum.



JEDEC#	MO-153AD			MO-153AD		
DWG#	PSS-24C			PSS-24C		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.045	0.046	0.047	1.14	1.17	1.20
A1	0.002	0.004	0.006	0.05	0.10	0.15
b	0.007	0.010	0.012	0.19	0.25	0.30
C	0.004	0.005	0.006	0.09	0.13	0.16
D	0.303	0.307	0.311	7.7	7.8	7.9
E	0.169	0.173	0.177	4.3	4.4	4.5
e	0.025 BSC			0.65 BSC		
H	0.238	0.252	0.269	6.1	6.4	6.7
L	0.020	0.024	0.030	0.50	0.60	0.75
N	24			24		
α	0°	5°	8°	0°	5°	8°
S	0.007	0.008	0.009	0.18	0.2	0.22

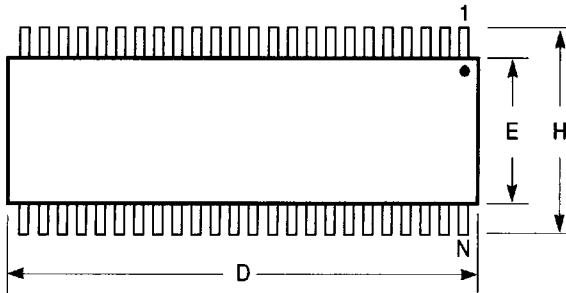
IN INCHES

IN MILLIMETERS

7466803 0003756 040

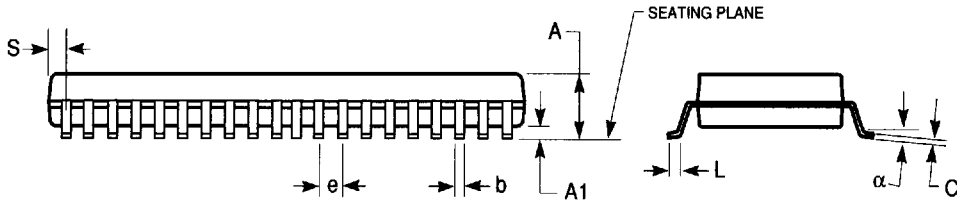
QUALITY SEMICONDUCTOR, INC.

240-MIL TSSOP - Package Code PA
Thin Shrink Small Outline Package
Plastic Small Outline Gull-Wing



Notes:

1. Refer to applicable symbol list.
2. N is the number of lead positions.
3. Dimensions D, E, and S are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
4. Lead coplanarity is 0.004in. maximum.



JEDEC#	MO-153ED			MO-153EE			MO-153ED			MO-153EE		
DWG#	PSS-48C			PSS-56C			PSS-48C			PSS-56C		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.039	0.043	0.047	0.039	0.043	0.047	1.00	1.10	1.20	1.00	1.10	1.20
A1	0.002	0.004	0.006	0.002	0.004	0.006	0.05	0.10	0.15	0.05	0.10	0.15
b	0.006	0.008	0.011	0.006	0.008	0.011	0.17	0.20	0.27	0.17	0.20	0.27
C	0.004	0.006	0.008	0.004	0.006	0.008	0.09	0.15	0.20	0.09	0.15	0.20
D	0.488	0.492	0.496	0.547	0.551	0.555	12.40	12.50	12.60	13.90	14.00	14.10
E	0.236	0.240	0.244	0.236	0.240	0.244	6.00	6.10	6.20	6.00	6.10	6.20
e	0.0197 BSC			0.0197 BSC			0.50 BSC			0.50 BSC		
H	0.315	0.319	0.323	0.315	0.319	0.323	8.00	8.10	8.20	8.00	8.10	8.20
L	0.018	0.024	0.030	0.018	0.024	0.030	0.45	0.60	0.75	0.45	0.60	0.75
N	48			56			48			56		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.015	0.020	0.025	0.006	0.010	0.014	0.38	0.50	0.65	0.15	0.25	0.35

DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETERS

7466803 0003757 T&T

QUALITY SEMICONDUCTOR, INC.