HARRIS SEMICONDUCTOR

CD74LCX16543

December 1997

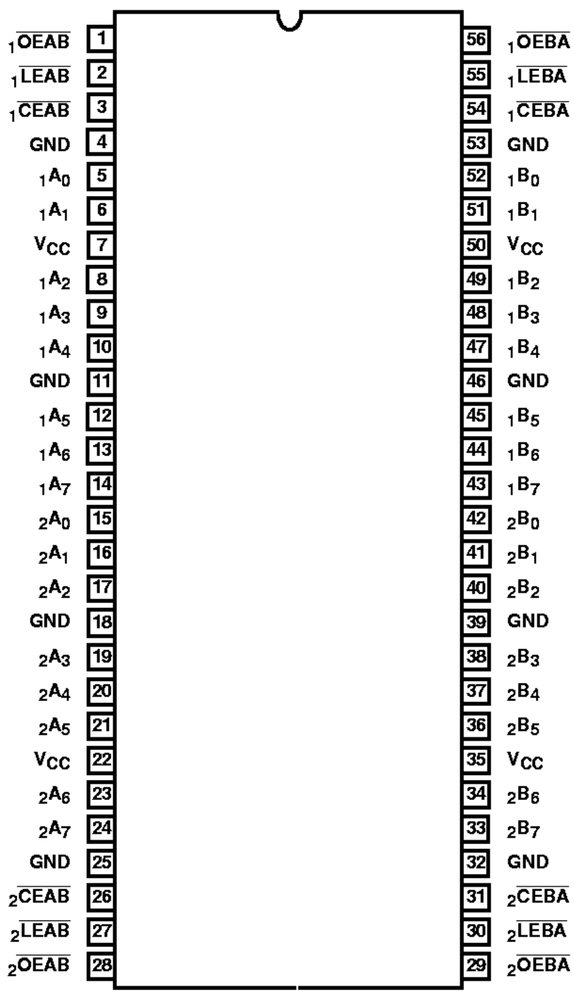
Fast CMOS 16-Bit Latched Transceiver

Features

- Advanced 0.6 micron CMOS Technology
- 5V Tolerant Inputs and Outputs
- Supports Live Insertion of PCBs
- 2.0V to 3.6V V_{CC} Supply Range
- Balanced 24mA Output Drive
- Low Ground Bounce Outputs
- ESD Protection Exceeds 2000V, HBM; 200V, MM
- Functionally Compatible with FCT3, LVC, LVT, and 74 Series Logic Families

Pinout

CD74LCX16543 (SSOP, TSSOP)
TOP VIEW



Description

Harris CD74LCX16543 is produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The CD74LCX16543 are 16-bit latched transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($_X\overline{CEAB}$) input must be LOW in order to enter data from xAx or to take data from xBx, as indicated in the Truth Table. With $_X\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the xLEAB signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $_X\overline{CEAB}$ and $_X\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $_X\overline{CEAB}$, $_X\overline{LEAB}$, and $_X\overline{OEAB}$ inputs.

The CD74LCX16543 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

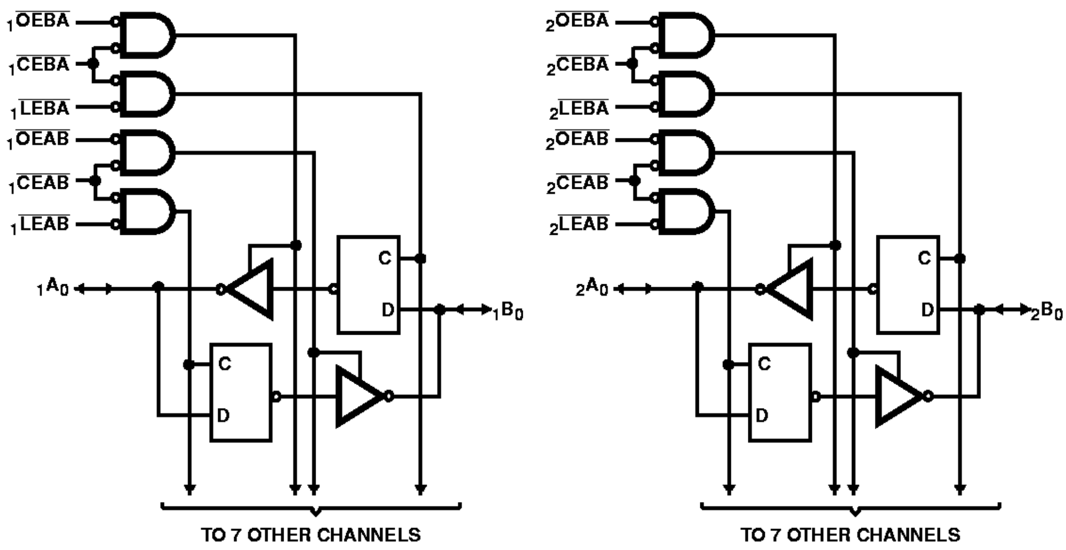
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD74LCX16543MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LCX16543SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4438**

Functional Block Diagram



TRUTH TABLE (NOTES 1, 3)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
${}_X\overline{CEAB}$	${}_X\overline{LEAB}$	${}_X\overline{OEAB}$	${}_XA_X$ TO ${}_XB_X$	${}_XB_X$
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 2)

NOTES:

1. A-to-B data flow is shown. B-to-A flow control is the same except using ${}_X\overline{CEBA}$, ${}_X\overline{LEBA}$, and ${}_X\overline{OEBA}$.
2. Before ${}_X$LEAB LOW-to-HIGH Transition
3. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
${}_X\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
${}_X\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
${}_X\overline{CEAB}$	A-to-B Enable Input (Active LOW)
${}_X\overline{CEBA}$	B-to-A Enable Input (Active LOW)
${}_X\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
${}_X\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
${}_XA_X$	A-to-B Data Inputs or B-to-A Three-State Outputs
${}_XB_X$	B-to-A Data Inputs or A -to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Temperature Range . . . . -40^oC to 85^oC
Supply Voltage to Ground Potential
Inputs and V_{CC} Only. . . . . -0.5V to 7.0V
Supply Voltage, V_{CC}
Operating . . . . 2.0V (Min), 3.6V (Max)
Data Retention . . . . 1.5V (Min), 3.6V (Max)
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} ($^oC/W$)
TSSOP Package 85
SSOP Package 70
Maximum Junction Temperature . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Output HIGH Voltage	V_{OH}	V_{CC} = 2.7V to 3.6V	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
		V_{CC} = 2.7V	I_{OH} = -12mA	2.2	-	-	V
		V_{CC} = 3.0V	I_{OH} = -18mA	2.4	-	-	V
			I_{OH} = -24mA	2.2	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = 2.7V to 3.6V	I_{OL} = 0.1mA	-	-	0.2	V
		V_{CC} = 2.7V	I_{OL} = 12mA	-	-	0.4	V
		V_{CC} = 3V	I_{OL} = 16mA	-	-	0.4	V
			I_{OL} = 24mA	-	-	0.55	V
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Input Current	I_I	V_{CC} = 2.7V to 3.6V	$0 \leq V_I \leq 5.5V$	-	-	±5	µA
High Impedance Output Current (Three-State)	I_{OZ}	V_{CC} = 2.7V to 3.6V	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}	-	-	±5	µA
Power Down Disable	I_{OFF}	V_{CC} = 0V	V_{IN} or $V_{OUT} \leq 5.5V$	-	-	10	µA
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 7)	-	-	500	µA
CAPACITANCE							
Input Capacitance (Note 8)	C_{IN}	V_{CC} = Open, V_{IN} = 0V or V_{CC}		-	7	-	pF
Output Capacitance (Note 8)	C_{OUT}	V_{CC} = 3.3V, V_{IN} = 0V or V_{CC}		-	8	-	pF
Power Dissipation Capacitance (Note 9)	C_{PD}	V_{CC} = 3.3V, V_{IN} = 0V or V_{CC}, f = 10MHz		-	20	-	pF

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V		UNITS
			MIN	MAX	MIN	MAX	
Propagation Delay A_n to B_n or B_n to A_n	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.2	1.5	6.0	ns
Propagation Delay $LEBA_n$ to A_n or $LEAB_n$ to B_n	t_{PLH}, t_{PHL}		1.5	6.5	1.5	7.5	ns
Output Enable Time $OEBA_n$ or $OEAB_n$ to A_n or B_n $CEBA_n$ or $CEAB_n$ to A_n or B_n	t_{PZH}, t_{PZL}		1.5	6.5	1.5	7.0	ns
Output Disable Time (Note 12) $OEBA_n$ or $OEAB_n$ to A_n or B_n $CEBA_n$ or $CEAB_n$ to A_n or B_n	t_{PHZ}, t_{PLZ}		1.5	6.5	1.5	7.0	ns
Setup Time HIGH or LOW, Data to $LExx_n$	t_S		2.5	-	2.5	-	ns
Hold Time HIGH or LOW, Data to $LExx_n$	t_H		1.5	-	1.5	-	ns
Pulse Width, Latch Enable, LOW	t_W		3.0	-	3.0	-	ns
Output to Output Skew (Note 13)	$t_{SK(0)}$		-	1.0	-	-	ns

Dynamic Switching Characteristics $T_A = 25^oC$

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	TYP	UNITS
Dynamic LOW Peak Voltage	V_{OLP}	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
Dynamic LOW Valley Voltage	V_{OLV}	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.8	V

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Per TTL driven input; all other inputs at V_{CC} or GND.
8. This parameter is determined by device characterization but is not production tested.
9. C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship: P_D (total power per latch) = $V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply range.
10. See test circuit and waveforms.
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. This parameter is guaranteed but not production tested.
13. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
14. Measured with n-1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.