Data Sheet | July 1999 | FN4613.1

Radiation Hardened Octal Three-State Transparent Latch

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil ACTS573T is a Radiation Hardened Octal Transparent Latch with an active low output enable. The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is High. When the latch goes low the data is latched. The output enable controls the three-state outputs. When the output enable pins ($\overline{OE}$) are high the output is in a high impedance state. The latch operation is independent of the state of output enable.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACTS573T are contained in SMD 5962-96725. For more information, visit our website at:
www.intersil.com/

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/

Ordering Information

ORDERING INFORMATION	PART NUMBER	TEMP. RANGE (^oC)
5962R9672502TRC	ACTS573DTR-02	-55 to 125
5962R9672502TXC	ACTS573KTR-02	-55 to 125

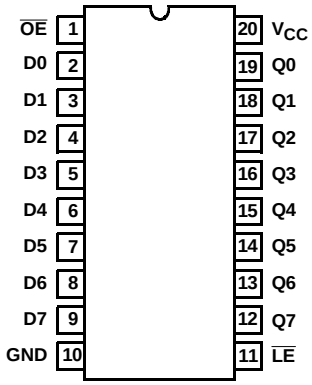
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct***.

Features

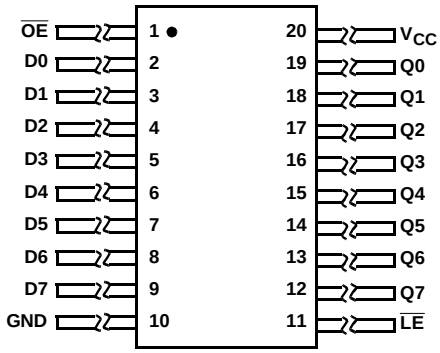
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions
  - Single Event Upset (SEU) Immunity: <1 x 10^{-10} Errors/Bit/Day (Typ)
  - SEU LET Threshold . . . . . .>100 MEV-cm^2/mg
- 1.25 Micron Radiation Hardened SOS CMOS
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- Input Logic Levels
  - V_{IL} = 0.8V Max
  - V_{IH} = VCC/2 Min
- Fast Propagation Delay . . . . . 18ns (Max), 12ns (Typ)

Pinouts

ACTS573T (SBDIP), CDIP2-T20
TOP VIEW

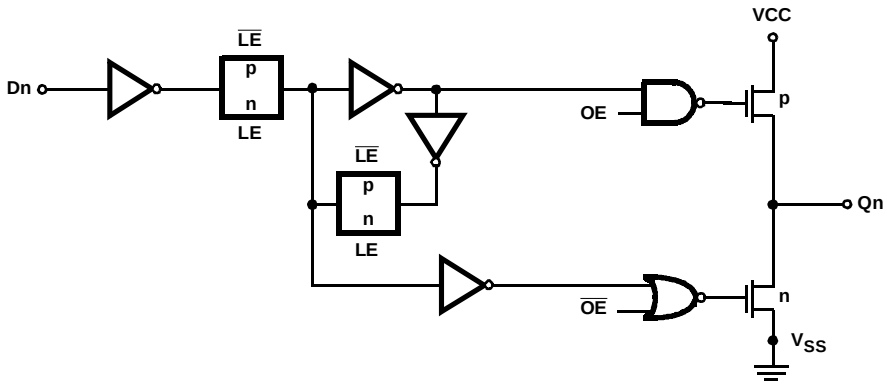


ACTS573T (FLATPACK), CDFP4-F20
TOP VIEW

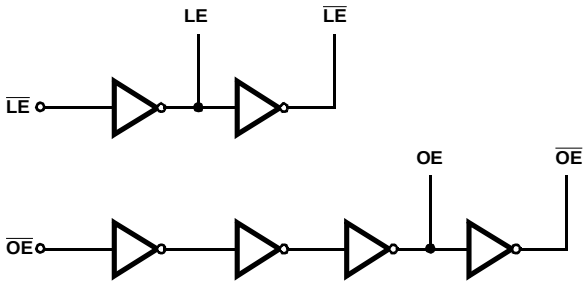


Functional Diagram

1 OF 8 IDENTICAL CIRCUITS



COMMON CONTROLS



TRUTH TABLE

$\overline{OE}$	$\overline{LE}$	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

NOTE: L = Low Logic Level, H = High Logic Level, X = Don't Care, Z = High Impedance, l = Low Voltage Level Prior to High-to-Low Latch Enable Transition, h = High Voltage Level Prior to High-to-Low Latch Enable Transition.

Die Characteristics

DIE DIMENSIONS:

(2600µm x 2600µm x 533µm ±51µm)

102 x 102 x 21mils ±2mil

METALLIZATION:

Type: Al Si Cu

Thickness: 10kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased (Silicon on Sapphire)

Bond Pad #20 First

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

190

PROCESS:

CMOS SOS

Metallization Mask Layout

ACTS573T