CMOS DUAL 4-BIT LATCH

FEATURES

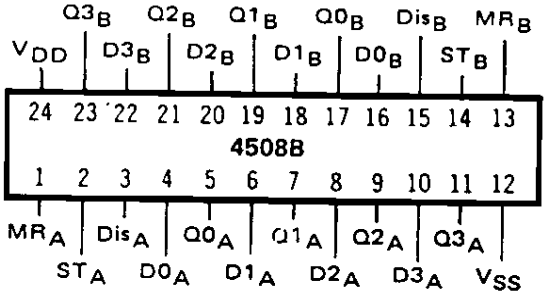
- Two Independent Four-Bit Latches
- 3-State Outputs
- Direct Reset
- All Inputs Buffered

DESCRIPTION

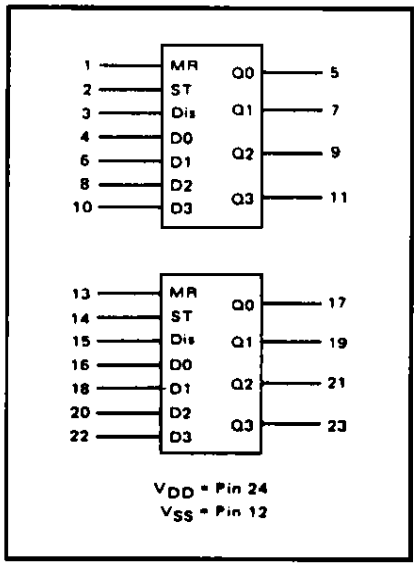
The 4508B consists of two identical independent 4-Bit Latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high-impedance state for bus line applications.

These devices find primary use in buffer storage, holding register, and display circuits, and other general digital logic applications.

CONNECTION DIAGRAM
(all packages)



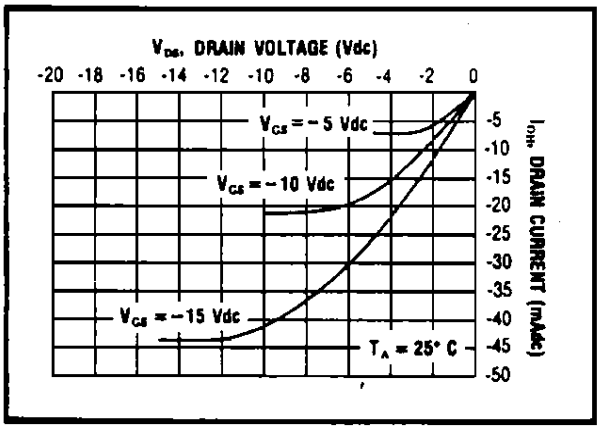
BLOCK DIAGRAM



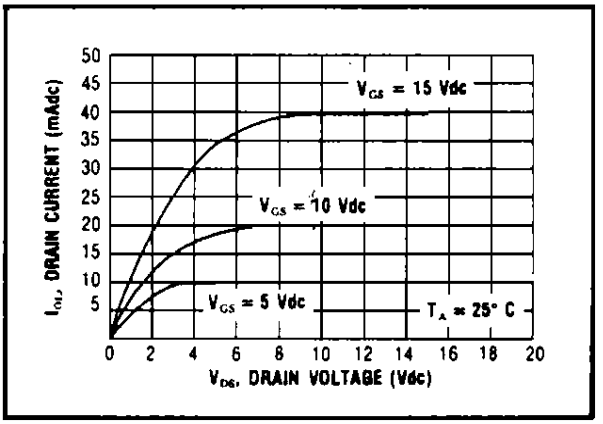
TRUTH TABLE

MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

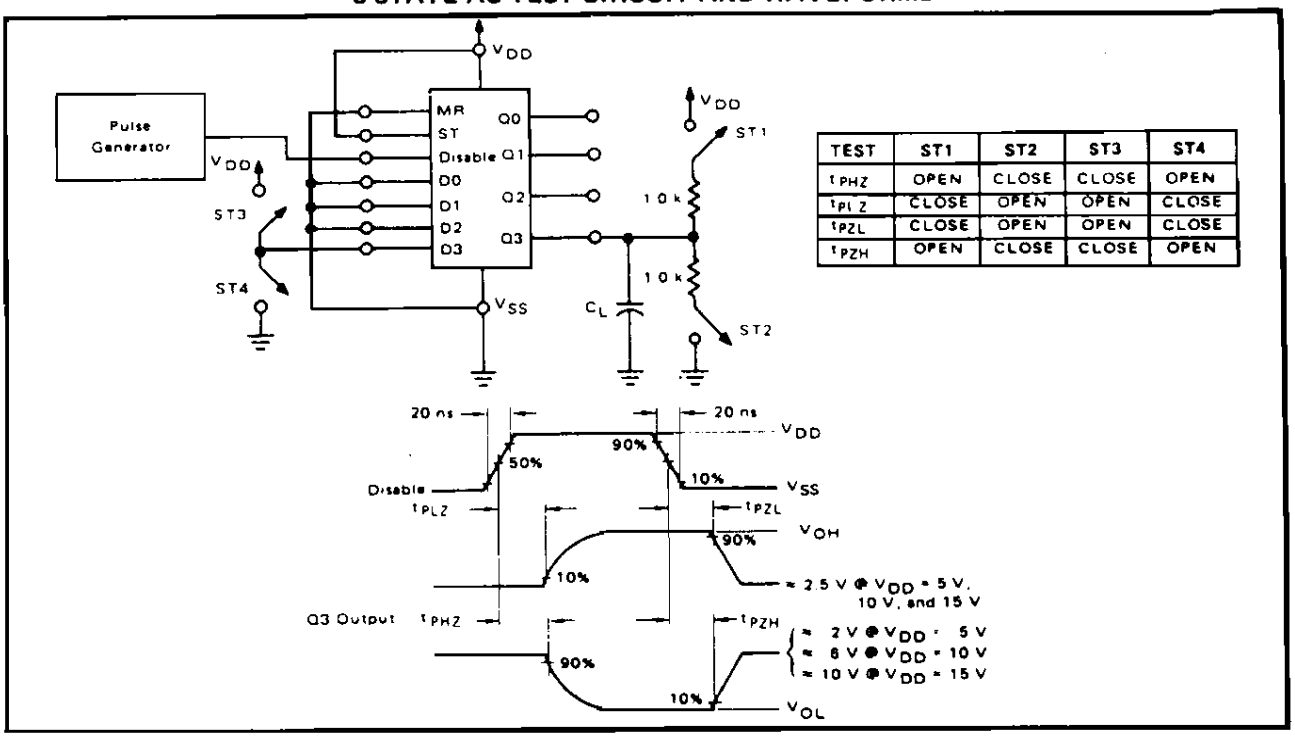
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}		+25°C			T_{HIGH}		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm 10^{-4}$	±0.1	–	±1.0	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t_{PLH}, t_{PHL}	5	–	220	440	ns
		10	–	90	180	
		15	–	60	120	
From Disable Input	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5	–	85	170	ns
		10	–	45	90	
		15	–	30	60	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM MASTER RESET PULSE WIDTH	PW_{MR}	5	–	100	200	ns
		10	–	50	100	
		15	–	35	70	
MINIMUM STROBE PULSE WIDTH	PW_{ST}	5	–	70	140	ns
		10	–	35	70	
		15	–	20	40	
MINIMUM SETUP TIME Data Inputs	t_{setup}	5	–	25	50	ns
		10	–	10	20	
		15	–	5	10	
MINIMUM HOLD TIME Data Inputs	t_{hold}	5	–	0	0	ns
		10	–	0	0	
		15	–	0	0	

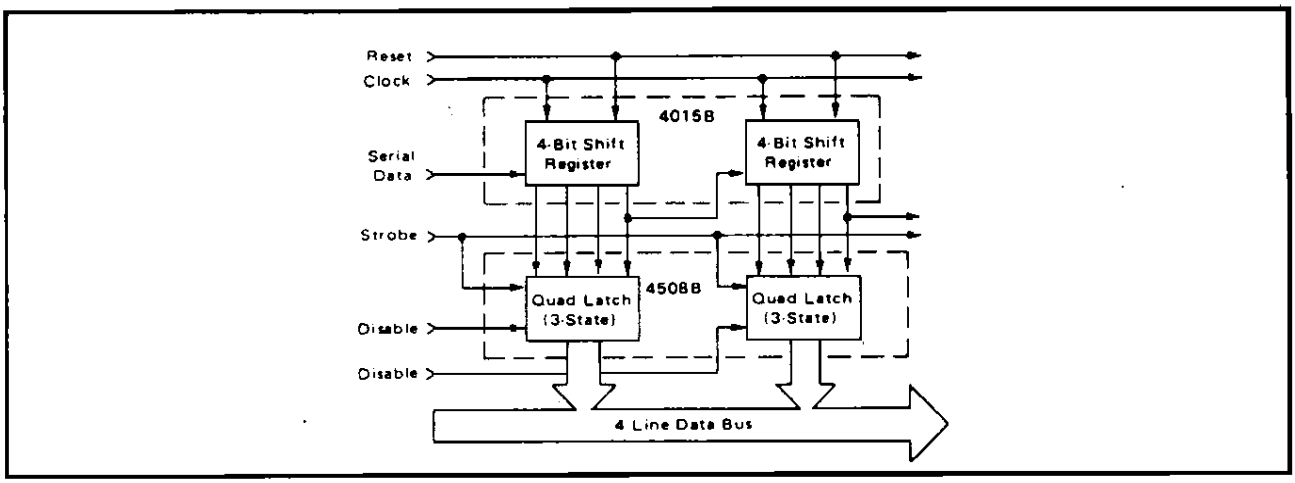
3-STATE AC TEST CIRCUIT AND WAVEFORMS



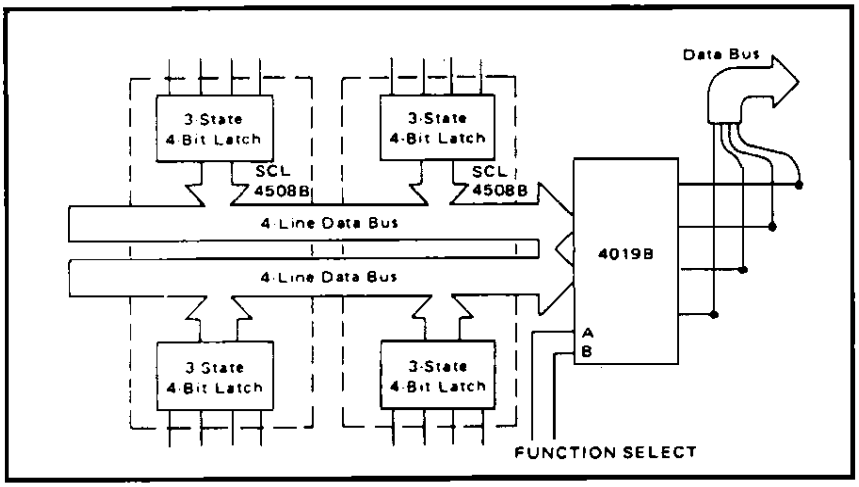
TEST	ST1	ST2	ST3	ST4
t_{PHZ}	OPEN	CLOSE	CLOSE	OPEN
t_{PLZ}	CLOSE	OPEN	OPEN	CLOSE
t_{PZL}	CLOSE	OPEN	OPEN	CLOSE
t_{PZH}	OPEN	CLOSE	CLOSE	OPEN

APPLICATIONS INFORMATION

BUS REGISTER



DUAL MULTIPLEXED BUS REGISTER WITH FUNCTION SELECT



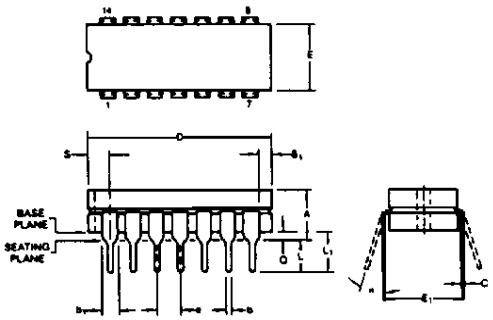
FUNCTION SELECT

A	B	Function
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	$A_i + B_i$

SCL4000B SERIES PACKAGE SPECIFICATIONS

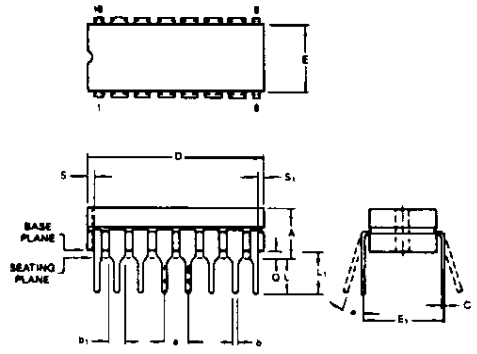
SUFFIX 'C' - CERAMIC GLASS FRIT SEAL DUAL IN LINE (CERDIP)

14 LEAD



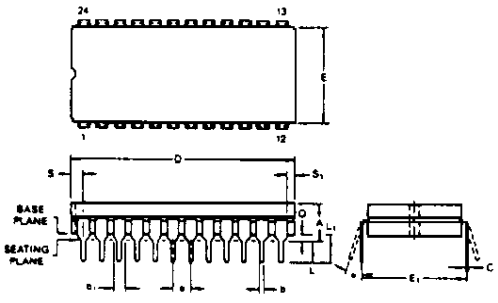
	Inches		Millimeters	
	Min	Max	Min	Max
A	—	0.200	—	5.080
Q	0.015	0.045	0.381	1.143
b	0.015	0.023	0.381	0.584
b_1	0.050	0.070	1.270	1.778
C	0.008	0.015	0.203	0.381
D	0.745	0.795	18.923	20.193
E	0.242	0.302	6.147	7.671
e	0.090	0.110	2.286	2.794
E_1	0.290	0.320	7.366	8.128
L	0.125	0.160	3.175	4.064
L_1	0.150	—	3.810	—
α	0-15°		0-15°	
S	—	0.098	—	2.489
S_1	0.025	—	0.635	—

16 LEAD



	Inches		Millimeters	
	Min	Max	Min	Max
A	—	0.200	—	5.080
Q	0.015	0.045	0.381	1.143
b	0.015	0.023	0.381	0.584
b_1	0.050	0.070	1.270	1.778
C	0.008	0.015	0.203	0.381
D	0.745	0.795	18.923	20.193
E	0.242	0.302	6.147	7.671
e	0.090	0.110	2.286	2.794
E_1	0.290	0.320	7.366	8.128
L	0.125	0.160	3.175	4.064
L_1	0.150	—	3.810	—
α	0-15°		0-15°	
S	—	0.060	—	1.524
S_1	0.005	—	0.127	—

24 LEAD



	Inches		Millimeters	
	Min	Max	Min	Max
A	—	0.200	—	5.080
Q	0.015	0.045	0.381	1.143
b	0.015	0.023	0.381	0.584
b_1	0.050	0.070	1.270	1.778
C	0.008	0.015	0.203	0.381
D	1.235	1.290	31.369	32.766
E	0.510	0.545	12.954	13.843
e	0.090	0.110	2.286	2.794
E_1	0.590	0.620	14.986	15.748
L	0.125	0.160	3.175	4.064
L_1	0.150	—	3.810	—
α	0-15°		0-15°	
S	—	0.098	—	2.489
S_1	0.025	—	0.635	—

SCL4000B SERIES FAMILY SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (VOLTAGE REFERENCED TO V_{SS})

PARAMETER		CONDITIONS	UNITS
DC SUPPLY VOLTAGE	V_{DD}	-0.5 to +18	Vdc
INPUT VOLTAGE	V_{IN}	-0.5 to V_{DD} +0.5	Vdc
DC INPUT CURRENT (ANY ONE INPUT)	I_{IN}	+/- 10	mAdc
POWER DISSIPATION	P_T	300	mW
STORAGE TEMPERATURE RANGE	T_S	-65 to +150	ºC

RECOMMENDED OPERATING CONDITIONS: (VOLTAGE REFERENCED TO V_{SS})

PARAMETER		CONDITIONS	UNITS
DC SUPPLY VOLTAGE	V_{DD}	3 to 15	Vdc
OPERATING TEMPERATURE RANGE	T_A		ºC
CERAMIC FRIT PACKAGE		-55 to +125	
DIE IN WAFFLE PACK		-55 to +125	
EPOXY MOLDED PACKAGE		-40 to +85	

PARAMETRIC LIMITS ARE GUARANTEED FOR V_{DD} = 5, 10, AND 15 Vdc. WHERE LOW POWER IS REQUIRED, THE SUPPLY VOLTAGE, CONSISTENT WITH REQUIRED SPEED SHOULD BE USED. FOR INCREASED NOISE IMMUNITY AND SPEED HIGHER SUPPLY VOLTAGES SHOULD BE SPECIFIED. THE LOWER LIMIT OF SUPPLY REGULATION IS 3 Vdc OR AS DETERMINED BY REQUIRED SYSTEM SPEED, NOISE IMMUNITY, OR, INTERFACE REQUIREMENTS. THE UPPER LIMIT IS 15Vdc OR AS DETERMINED BY POWER DISSIPATION RESTRICTIONS OR INTERFACE REQUIREMENTS. UNUSED INPUTS MUST BE CONNECTED TO V_{DD} , V_{SS} OR ANOTHER INPUT. ALWAYS USE PRECAUTIONS TO PROTECT AGAINST STATIC CHARGES.

SCL4000B SERIES FAMILY SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

PARAMETRIC LIMITS LISTED HERE ARE GUARANTEED FOR THE ENTIRE SCL4000B SERIES FAMILY UNLESS OTHERWISE SPECIFIED ON THE DEVICE DATA SHEETS.

STATIC CHARACTERISTICS: (V_{SS} = 0 V)

PARAMETER	CONDITIONS	V_{DD} (Vdc)	T_{LOW}* MIN	T_{LOW}* MAX	+25°C MIN	+25°C TYP	+25°C MAX	T_{HIGH}** MIN	T_{HIGH}** MAX	UNIT
QUIESCENT DEVICE CURRENT I_{DD}										
GATES	V_{IN} = V_{SS} OR V_{DD}	5		0.05		0.0005	0.05		1.5	µAdc
		10		0.1		0.001	0.1		3.0	
		15		0.2		0.002	0.2		6.0	
BUFFERS, FLIP-FLOPS	ALL VALID INPUT COMBINATIONS.	5		1.0		0.005	1.0		30	µAdc
		10		2.0		0.01	2.0		60	
		15		4.0		0.02	4.0		120	
MSI		5		5		0.05	5		150	µAdc
		10		10		0.1	10		300	
		15		20		0.2	20		600	
HIGH-LEVEL OUTPUT VOLTAGE V_{OH}	V_{IN} = V_{SS} OR V_{DD} $\lvert I_O \rvert \leq 1\mu A$	5	4.99		4.99	5		4.95		Vdc
		10	9.99		9.99	10		9.95		
		15	14.99		14.99	15		14.95		
LOW-LEVEL OUTPUT VOLTAGE V_{OL}	V_{IN} = V_{SS} OR V_{DD} $\lvert I_O \rvert \leq 1\mu A$	5		0.01		0	0.01		0.05	Vdc
		10		0.01		0	0.01		0.05	
		15		0.01		0	0.01		0.05	
MINIMUM INPUT HIGH VOLTAGE V_{IH}	V_O = 0.5V OR 4.5V	5		3.5		2.75	3.5		3.5	Vdc
	V_O = 1.0V OR 9.0V	10		7.0		5.5	7.0		7.0	
	V_O = 1.5V OR 13.5V	15		11.0		8.25	11.0		11.0	
MAXIMUM INPUT LOW VOLTAGE V_{IL}	V_O = 0.5V OR 4.5V	5	1.5		1.5	2.25		1.5		Vdc
	V_O = 1.0V OR 9.0V	10	3.0		3.0	4.5		3.0		
	V_O = 1.5V OR 13.5V	15	4.0		4.0	6.75		4.0		
INPUT CURRENT I_{IN}	V_{IN} = 0 OR 15 V	15		± 0.1		$\pm 10^{-5}$	± 0.1		± 1.0	µAdc
OUTPUT LOW CURRENT (B REV) I_{OL} V_{IN} = V_{SS} OR V_{DD}	V_{OL} = 0.4V	5	0.64		0.51	1.25		0.36		mAdc
	V_{OL} = 0.5V	10	1.6		1.3	3.25		0.9		
	V_{OL} = 1.5V	15	4.2		3.4	10		2.4		
OUTPUT HIGH CURRENT (B REV) I_{OH} V_{IN} = V_{SS} OR V_{DD}	V_{OH} = 4.6V	5	-0.64		-0.51	-1.25		-0.36		mAdc
	V_{OH} = 9.5V	10	-1.6		-1.3	-3.25		-0.9		
	V_{OH} = 13.5V	15	-4.2		-3.4	-10		-2.4		
OUTPUT HIGH CURRENT† I_{OH} V_{IN} = V_{SS} OR V_{DD}	V_{OH} = 4.6V	5	-0.25		-0.2			-0.14		mAdc
	V_{OH} = 9.5V	10	-0.62		-0.5			-0.35		
	V_{OH} = 13.5V	15	-1.8		-1.5			-1.1		

SCL4000B SERIES FAMILY SPECIFICATIONS

STATIC CHARACTERISTICS‡: (V_{SS} = 0 V)

PARAMETER	CONDITIONS	V_{DD} (Vdc)	T_{LOW}* MIN	T_{LOW}* MAX	+25°C MIN	+25°C TYP	+25°C MAX	T_{HIGH}** MIN	T_{HIGH}** MAX	UNITS
MINIMUM INPUT HIGH VOLTAGE V_{IH}	V_O = 0.5V OR 4.5V	5		4.0		2.75	4.0		4.0	
	V_O = 1.0V OR 9.0V	10		8.0		5.5	8.0		8.0	Vdc
	V_O = 1.5V OR 13.5V	15		12.0		8.25	12.0		12.0	
MAXIMUM INPUT LOW VOLTAGE V_{IL}	V_O = 0.5V OR 4.5V	5	1.0		1.0	2.25		1.0		
	V_O = 1.0V OR 9.0V	10	2.0		2.0	4.5		2.0		Vdc
	V_O = 1.5V OR 13.5V	15	3.0		3.0	6.75		3.0		

DYNAMIC CHARACTERISTICS: (T_A = 25 ° C)

PARAMETER	V_{DD} (Vdc)	MINIMUM	TYPICAL	MAXIMUM	UNIT
INPUT CAPACITANCE C_{IN}			7.5		pF

NOTES:

* T_{LOW} = -55 ºC FOR C, C+, and, HN DEVICES
-40 ºC FOR E, and, S DEVICES

** T_{HIGH} = + 125 ºC FOR C, C+, and, HN DEVICES
+ 85 ºC FOR E, and, S DEVICES

† THIS SPECIFICATION APPLIES ONLY TO THE BELOW LISTED DEVICE TYPES:

4018B, 4024B, 4029B, 4035B, 4402B, 4412B, 4428B, 4510B, 4512B, 4514B, 4515B, 4516B, 4527B, 4528B, 4531B, 4555B, 4556B, 4581B, 4582B, 4585B.

‡ THIS SPECIFICATION APPLIES ONLY TO THE BELOW LISTED DEVICE TYPES:

4001UB, 4007UB, 4009UB, 4011UB, 4041UB, 4049UB, 4069UB, 4441UB, 4449UB.

MARKING INFORMATION

SCL	**4xxxB**	**C**	**•**
Family Type	**Device Type**	**Package Type**	**Screening Level**
Standard CMOS Logic	**Consists of four numerals & one or two letters.**	**C = CERDIL**	**• = Standard Test**
		E = PDIL	**+ = Plus Tested Enhanced Screening**
		S = SMD/SOIC	**L = High Reliability Screening**

SCL4000B SERIES CERDIP PRODUCT FLOW

This product flow applies to all 14, 16, and 24 lead ceramic dual-in-line packaged products with a glass-frit hermetic seal (Cerdip).

Product Flow Step	Mil Grade Cerdip Suffix CL	Enhanced Cerdip Suffix C+	Standard Cerdip Suffix C
Wafer Fabrication	Identical Circuit Design and Wafer Fabrication Processes		
Wafer Probe	100% Probe with Identical Test Programs		
Optical Inspection	100% to Mil Std 883 Method 2010 B		
QC Optical Inspection	Mil Std 883 Method 2010 B 0.65% AQL II		
Die Attach	Glass		
Temperature Cycle	100% Ten Cycles -65ºC to +150 C		
Centrifuge	100% 30kg Method 2001 Y1 Direction		
Tin Plate	400 to 1000 Microns	300 to 800 Microns	300 to 800 Microns
Solder Dip	200 Microns	Not Applicable	Not Applicable
Marking	Markem 7224 White		
Fine Leak	100% to Mil Std 883 Method 1014 B		
Gross Leak	100% to Mil Std 883 Method 1014 C		
Test	100% DC at 25ºC		
Burn-in	100% Static Burn-in 168 Hours at 125ºC Or Equivalent	100% Static Burn-in 168 Hours at 125ºC Or Equivalent	Not Applicable
Post Test	100% DC at 25ºC	100% DC at 25ºC	Not Applicable
QC Inspection	DC at 25ºC LTPD 3% C=0 PDA 10%	DC at 25ºC LTPD 3% C=0 PDA 10%	Not Applicable
High Temperature Test	100% DC at 125ºC	Not Applicable	Not Applicable
QC Inspection	DC at 55ºC DC at 125ºC LTPD 3% C=0	Not Applicable	Not Applicable
Final QC Inspection	Fine and Gross Leak LTPD 5% C=0		
	DC at 25ºC 0.065% AQL II		
	Visual Inspection 0.65% AQL II		

Product Flow Comparison - BCL vs 883

This product flow chart compares the *R&E* SCL4000BCL product flow to an 883 fully compliant product flow.

Product Flow Step	SCL4xxxBCL	883
Wafer Fabrication	Identical Circuit Design and Wafer Fabrication Process	
Wafer Probe	100% Probe with Identical Test Programs	
Assembly	Glass Die Attach	Gold Die Attach
Test	100% DC at 25ºC with Identical Test Programs	
Post Room PDA	10%	5%
High LTPD	3%	2%
-55 C Production Test	Not Performed	100%
-55 C LTPD	5%	2%
AC Production Test	Not Performed	100%
AC LTPD	Not Performed	2%
Final Visual	Sampled	100%
Group Testing	Not Performed	A, B, C, D

LTPD Sample Plans

Plan	Sample Size	Allowable Rejects
2%	116	0
3%	76	0
5%	45	0