54F/74F373

Octal Transparent Latch With 3-State Outputs

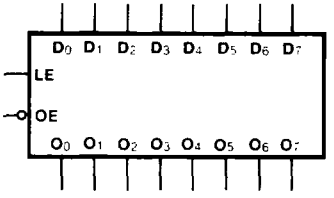
Description

The 'F373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

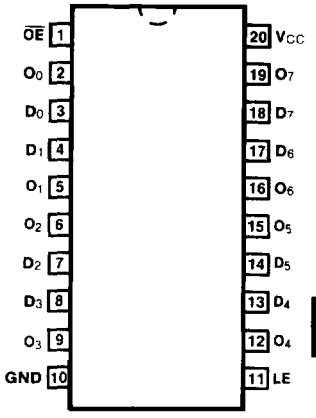
- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**

Ordering Code: See Section 5

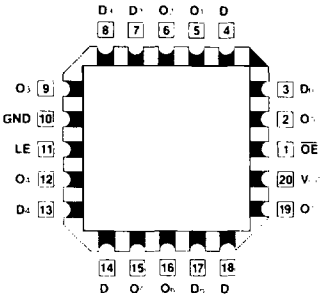
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

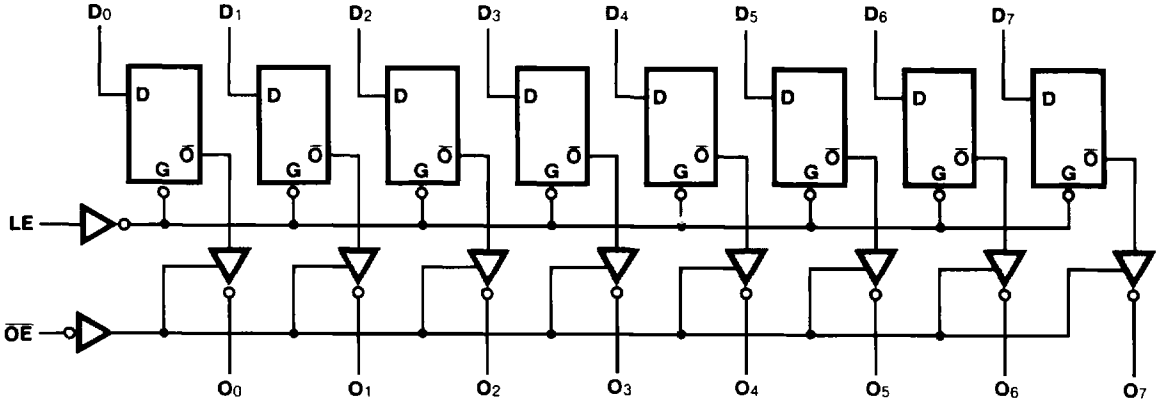
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
O_0-O_7	3-State Latch Outputs	75/15 (12.5)

Functional Description

The 'F373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		38	55	mA	V_{CC} = Max, $\overline{OE}$ = HIGH D_n, LE = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$ $C_L = 50\,pF$			T_A, V_{CC} = Mil $C_L = 50\,pF$		T_A, V_{CC} = Com $C_L = 50\,pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	5.3	7.0	3.0	8.5	3.0	8.0	ns	3-1
t_{PHL}	D_n to O_n	2.0	3.7	5.0	2.0	7.0	2.0	6.0		3-4
t_{PLH}	Propagation Delay	5.0	9.0	11.5	5.0	15.0	5.0	13.0	ns	3-1
t_{PHL}	LE to O_n	3.0	5.2	7.0	3.0	8.5	3.0	8.0		3-7
t_{PZH}	Output Enable Time	2.0	5.0	11.0	2.0	13.5	2.0	12.0	ns	3-1, 3-12
t_{PZL}		2.0	5.6	7.5	2.0	10.0	2.0	8.5		3-13
t_{PHZ}	Output Disable Time	2.0	4.5	6.5	2.0	10.0	2.0	7.5	ns	3-1, 3-12
t_{PLZ}		2.0	3.8	6.0	2.0	7.0	2.0	6.0		3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	2.0			2.0		2.0		ns	3-15
$t_s(L)$	D_n to LE	2.0			2.0		2.0			
$t_h(H)$	Hold Time, HIGH or LOW	3.0			3.0		3.0			
$t_h(L)$	D_n to LE	3.0			3.0		3.0			
$t_w(H)$	LE Pulse Width, HIGH	6.0			6.0		6.0		ns	3-7