

DATA SHEET

74LVC373

Octal D-type transparent latch (3-State)

Product specification
Supersedes data of February 1996
IC24 Data Handbook

1997 Mar 18

Octal D-type transparent latch (3-State)

74LVC373

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Common 3-State output enable input
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC373 is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable (\overline{OE}) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the eight latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The '373' is functionally identical to the '573', but the '573' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|---|---|------------|------|
| t_{PHL}/t_{PLH} | Propagation delay Dn to Qn LE to Qn | $C_L = 50\text{pF}$ $V_{CC} = 3.3\text{V}$ | 4.3 4.6 | ns |
| C_I | Input capacitance | | 5.0 | pF |
| C_{PD} | Power dissipation capacitance per latch | Notes 1, 2 | 23 | pF |

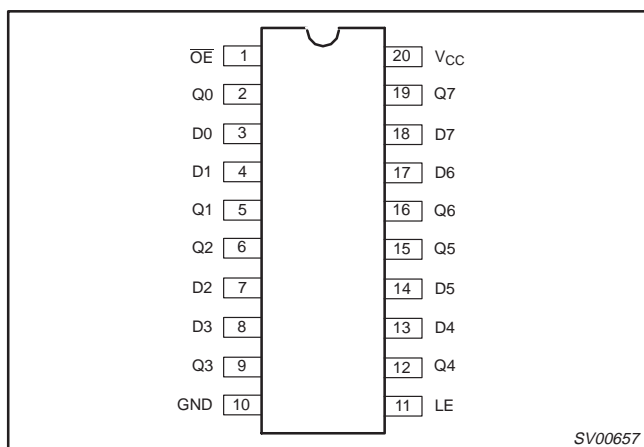
NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
- The condition is $V_I = \text{GND to } V_{CC}$.

ORDERING AND PACKAGE INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG. DWG. # |
|-----------------------------|-------------------|-----------------------|---------------|-------------|
| 20-Pin Plastic SO | -40°C to +85°C | 74LVC373 D | 74LVC373 D | SOT163-1 |
| 20-Pin Plastic SSOP Type II | -40°C to +85°C | 74LVC373 DB | 74LVC373 DB | SOT339-1 |
| 20-Pin Plastic TSSOP Type I | -40°C to +85°C | 74LVC373 PW | 74LVC373PW DH | SOT360-1 |

PIN CONFIGURATION



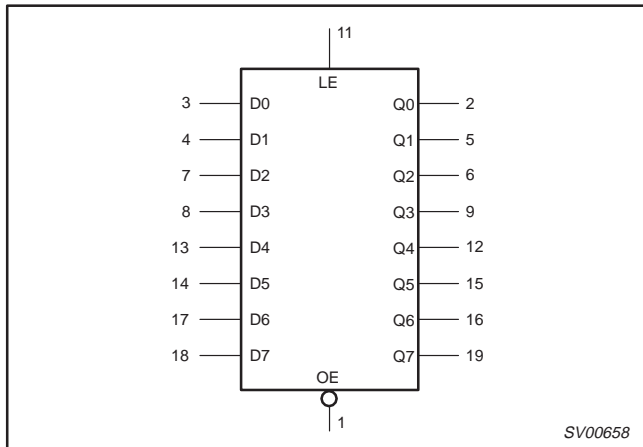
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|----------------------------|-----------------|----------------------------------|
| 1 | \overline{OE} | Output enable input (active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0–Q7 | 3-State latch outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0–D7 | Data inputs |
| 10 | GND | Ground (0V) |
| 11 | LE | Latch enable input (active HIGH) |
| 20 | V_{CC} | Positive supply voltage |

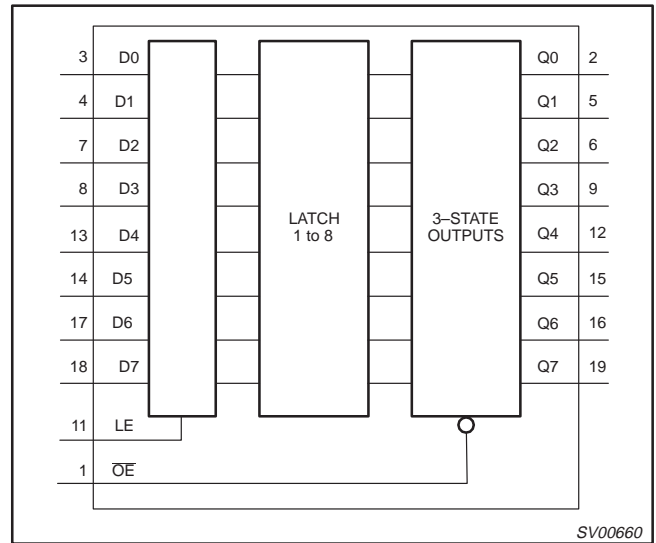
Octal D-type transparent latch (3-State)

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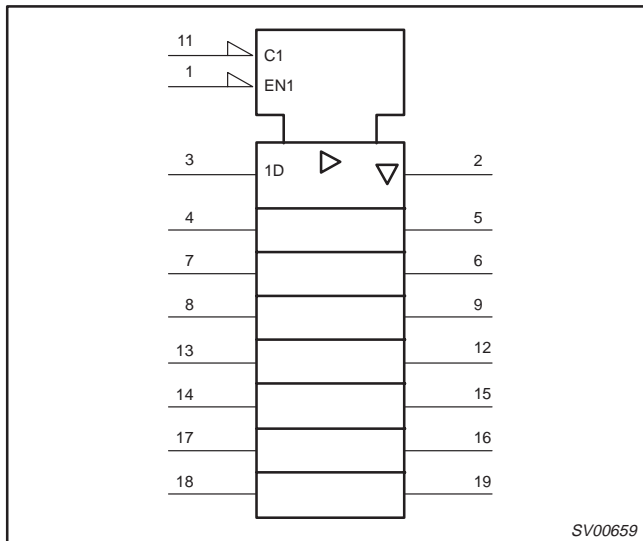
LOGIC SYMBOL



FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)

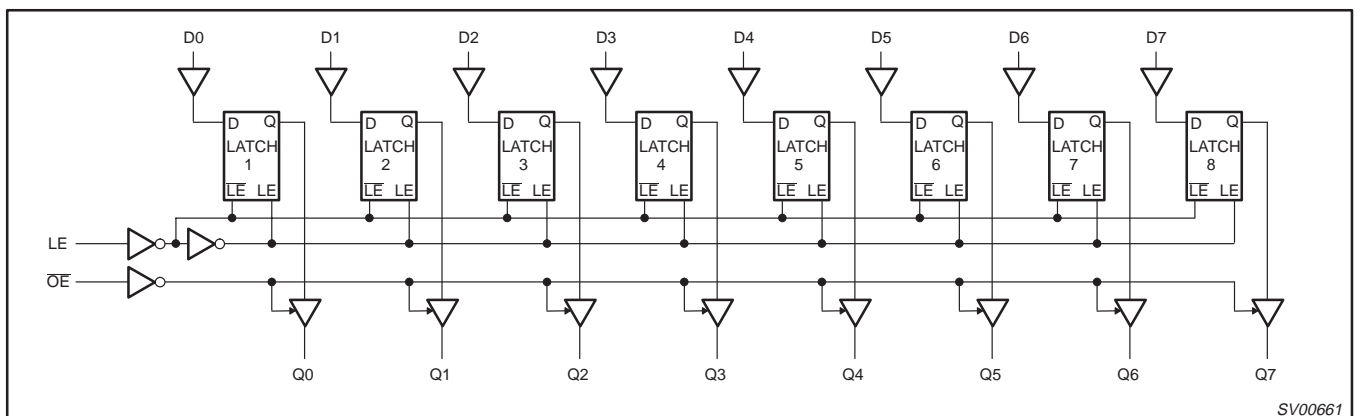


FUNCTION TABLE

| OPERATING MODES | INPUTS | | | INTERNAL LATCHES | OUTPUTS Q0 to Q7 |
|---|-----------------|--------|--------|------------------|---------------------|
| | \overline{OE} | LE | Dn | | |
| Enable and read register (transparent mode) | L L | H H | L H | L H | L H |
| Latch and read register | L L | L L | l h | L H | L H |
| Latch register and disable outputs | H H | L L | l h | L H | Z Z |

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
 X = Don't care
 Z = High impedance OFF-state

LOGIC DIAGRAM



Octal D-type transparent latch (3-State)

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|------------|--|--|--------|----------|------|
| | | | MIN | MAX | |
| V_{CC} | DC supply voltage (for max. speed performance) | | 2.7 | 3.6 | V |
| V_{CC} | DC supply voltage (for low-voltage applications) | | 1.2 | 3.6 | V |
| V_I | DC input voltage range | | 0 | 5.5 | V |
| $V_{I/O}$ | DC input voltage range for I/Os | | 0 | V_{CC} | V |
| V_O | DC output voltage range | | 0 | V_{CC} | V |
| T_{amb} | Operating free-air temperature range | | -40 | +85 | °C |
| t_p, t_f | Input rise and fall times | $V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$ | 0 0 | 20 10 | ns/V |

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|-------------------|--|--|------------------------|------|
| V_{CC} | DC supply voltage | | -0.5 to +6.5 | V |
| I_{IK} | DC input diode current | $V_I < 0$ | -50 | mA |
| V_I | DC input voltage | Note 2 | -0.5 to +5.5 | V |
| $V_{I/O}$ | DC input voltage range for I/Os | | -0.5 to $V_{CC} + 0.5$ | V |
| I_{OK} | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | ± 50 | mA |
| V_{OUT} | DC output voltage | Note 2 | -0.5 to $V_{CC} + 0.5$ | V |
| I_{OUT} | DC output source or sink current | $V_O = 0$ to V_{CC} | ± 50 | mA |
| I_{GND}, I_{CC} | DC V_{CC} or GND current | | ± 100 | mA |
| T_{stg} | Storage temperature range | | -60 to +150 | °C |
| P_{TOT} | Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP) | above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K | 500 500 | mW |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|------------------------------------|---|---|-----------------------|------------------|------|------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V _{IH} | HIGH level Input voltage | V _{CC} = 1.2V | V _{CC} | | | V |
| | | V _{CC} = 2.7 to 3.6V | 2.0 | | | |
| V _{IL} | LOW level Input voltage | V _{CC} = 1.2V | | | GND | V |
| | | V _{CC} = 2.7 to 3.6V | | | 0.8 | |
| V _{OH} | HIGH level output voltage | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA | V _{CC} - 0.5 | | | V |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA | V _{CC} - 0.2 | V _{CC} | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA | V _{CC} - 0.6 | | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA | V _{CC} - 1.0 | | | |
| V _{OL} | LOW level output voltage | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA | | | 0.40 | V |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA | | GND | 0.20 | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA | | | 0.55 | |
| I _I | Input leakage current | V _{CC} = 3.6V; V _I = 5.5V or GND Not for I/O pins | | ± 0.1 | ± 5 | μA |
| I _{IHZ} /I _{ILZ} | Input current for common I/O pins | V _{CC} = 3.6V; V _I = V _{CC} or GND | | ± 0.1 | ± 15 | μA |
| I _{OZ} | 3-State output OFF-state current | V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND | | 0.1 | ± 10 | μA |
| I _{CC} | Quiescent supply current | V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0 | | 0.1 | 20 | μA |
| ΔI _{CC} | Additional quiescent supply current per input pin | V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0 | | 5 | 500 | μA |

NOTE:1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.**AC CHARACTERISTICS**GND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | | UNIT |
|------------------------------------|---|--------------|-------------------------------|------------------|-----|------------------------|-----|------------------------|------|
| | | | V _{CC} = 3.3V ± 0.3V | | | V _{CC} = 2.7V | | V _{CC} = 1.2V | |
| | | | MIN | TYP ¹ | MAX | MIN | MAX | TYP | |
| t _{PHL} /t _{PLH} | Propagation delay Dn to Qn | Figures 1, 5 | 1.5 | 4.3 | 8.0 | 1.5 | 9.0 | 21 | ns |
| t _{PHL} /t _{PLH} | Propagation delay LE to Qn | Figures 2, 5 | 1.5 | 4.6 | 9.0 | 1.5 | 10 | 23 | ns |
| t _{PZH} /t _{PZL} | 3-State output enable time OE to Qn | Figures 3, 5 | 1.5 | 3.8 | 8.5 | 1.5 | 9.5 | 17 | ns |
| t _{PHZ} /t _{PLZ} | 3-State output disable time OE to Qn | Figures 3, 5 | 1.5 | 3.5 | 7.5 | 1.5 | 8.5 | 8.0 | ns |
| t _W | LE pulse width HIGH | Figure 2 | 4.0 | 3.0 | – | 4.0 | – | – | ns |
| t _{SU} | Set-up time Dn to LE | Figure 4 | 2.0 | 0.4 | – | 3.0 | – | – | ns |
| t _H | Hold time Dn to LE | Figure 4 | 2.0 | 0 | – | 3.0 | – | – | ns |

NOTE:1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5V * V_{CC}$ at $V_{CC} < 2.7V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$

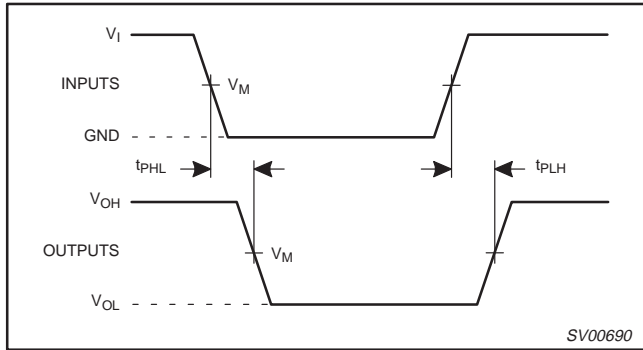


Figure 1. Input (Dn) to output (Qn) propagation delays

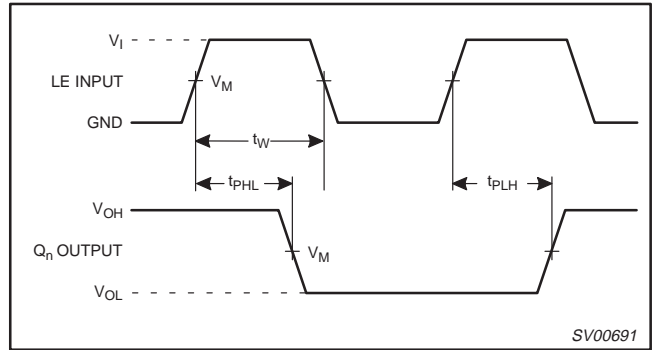


Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays

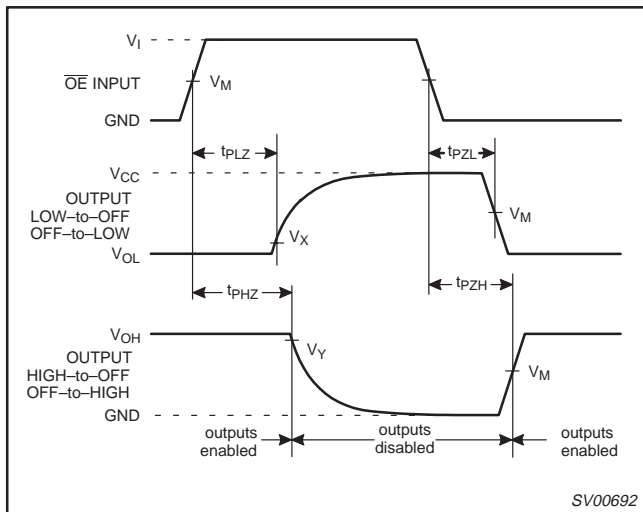


Figure 3. 3-State enable and disable times

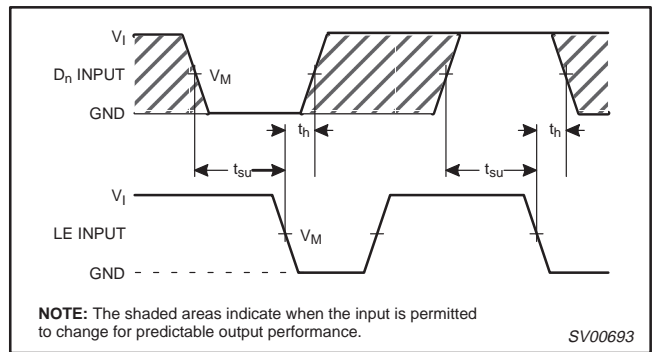


Figure 4. Data set-up and hold times for the Dn input to the LE input

TEST CIRCUIT

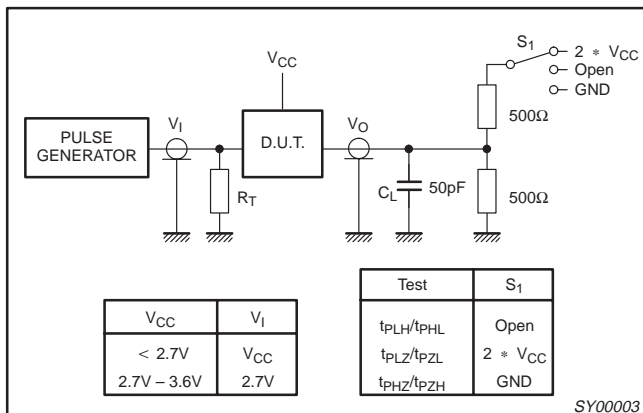


Figure 5. Load circuitry for switching times

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 13.0 12.6 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.51 0.49 | 0.30 0.29 | 0.050 | 0.42 0.39 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013AC | | | | 92-11-17 95-01-24 |

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2.0 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 7.4 7.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 0.9 0.5 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT339-1 | | MO-150AE | | | | 93-09-08 95-02-04 |

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.10 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 6.6 6.4 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1.0 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.5 0.2 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|-----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT360-1 | | MO-153AC | | | | -93-06-16 95-02-04 |

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
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