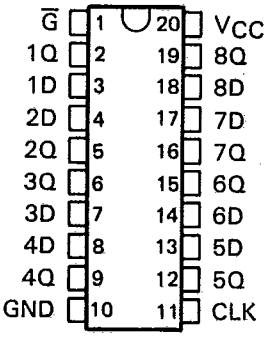
SN54F377, SN74F377
OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

D2932, MARCH 1987—REVISED SEPTEMBER 1989

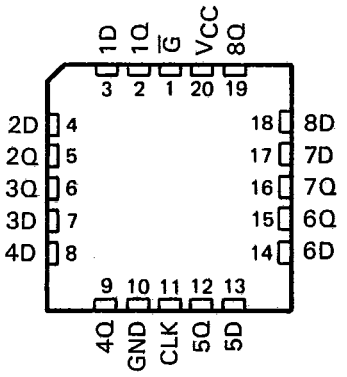
- **Contains Eight D-Type Flip-Flops with Single-Rail Outputs**
- **Buffered Common Enable Input**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Register
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F377 . . . J PACKAGE
SN74F377 . . . DW OR N PACKAGE
(TOP VIEW)

T-46-07-11



SN54F377 . . . FK PACKAGE
(TOP VIEW)



description

The SN54F377 and SN74F377 are monolithic, positive-edge-triggered D-type flip-flops with a clock enable input. The 'F377 is similar to the 'F273, but features a common clock enable instead of a common clear.

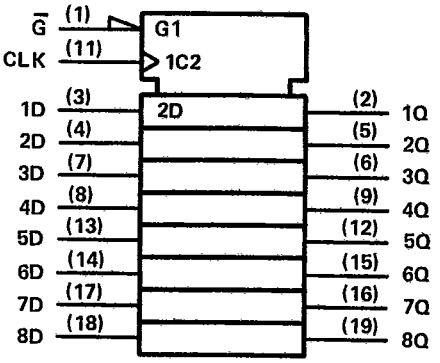
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the clock enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{G}$ input.

The SN54F377 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F377 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{G}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

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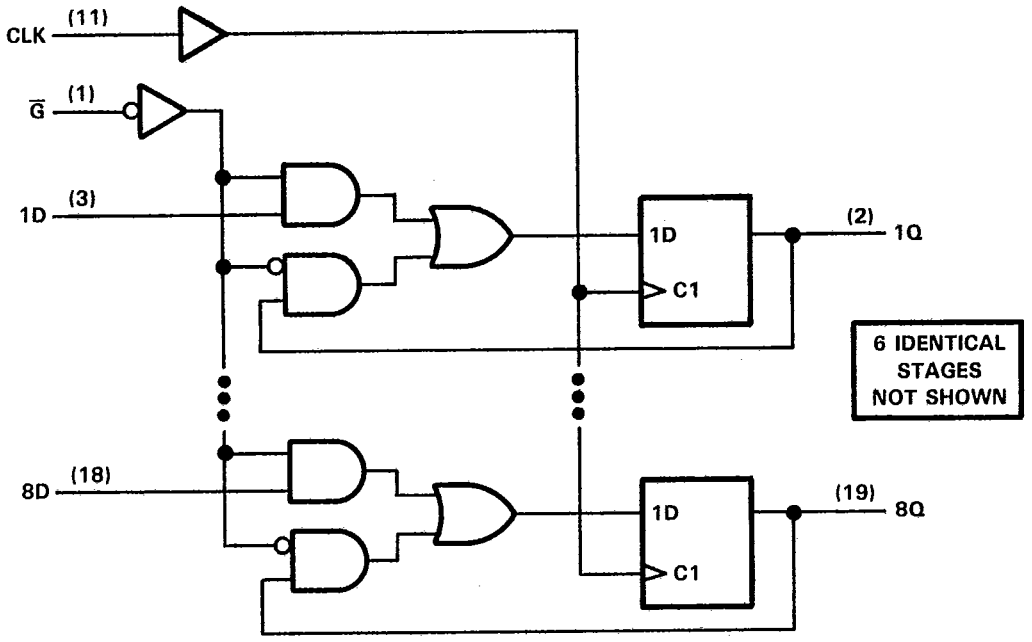
logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F377 . . . . . −55°C to 125°C
SN74F377 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F377			SN74F377			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F377			SN74F377			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 0,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	See Note 1		55	72		55	72	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 2		70	90		70	90	mA

timing requirements

			V_{CC} = 5 V, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§		UNIT
			'F377	SN54F377	SN74F377	
			MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency		0 110	0	100	MHz
t_{su}	Setup time before CLK↑	Data high or low	2		2	ns
t_h	Hold time after CLK↑	Data high or low	1		1	ns
t_{su}	Setup time before CLK↑	$\overline{G}$ high	2.5		2.5	ns
		$\overline{G}$ low	3		3	
t_h	Hold time after CLK↑	$\overline{G}$ high or low	0		0	ns
t_w	Pulse duration	CLK low	4		5	ns

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§			UNIT
			'F377			SN54F377		SN74F377	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			110	125				100		MHz
t_{PLH}	CLK	Any Q	4	6.5	8.5			4	10	ns
t_{PHL}			4	7	9			4	10.5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ No more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 1. I_{CC} is measured after applying a momentary ground, then 4.5 V, to the clock input with all data inputs at 4.5 V and the enable input at ground.
2. I_{CCL} is measured after applying a momentary ground, then 4.5 V, to the clock input with all data and enable inputs at ground.
3. Load circuits and waveforms are shown in Section 1 of the *F Logic (SN54/74F) Data Book, 1989.*