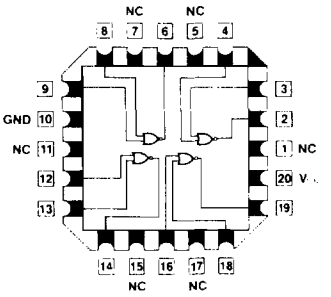
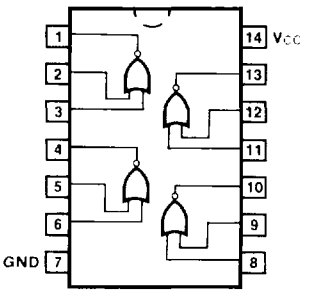
54F/74F02

Quad 2-Input NOR Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		3.7	5.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			8.7	13.0		*	

*Measured with one input HIGH, one input LOW for each gate.

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	2.5 1.5	4.4 3.2	5.5 4.3	2.5 1.5	7.5 6.5	2.5 1.5	6.5 5.3	ns	3-1 3-3