Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BUS TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT, BUS-HOLD

IDT74LVCH162646A
ADVANCE INFORMATION

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH162646A:

- Balanced Output Drivers: ±12mA
- Low switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

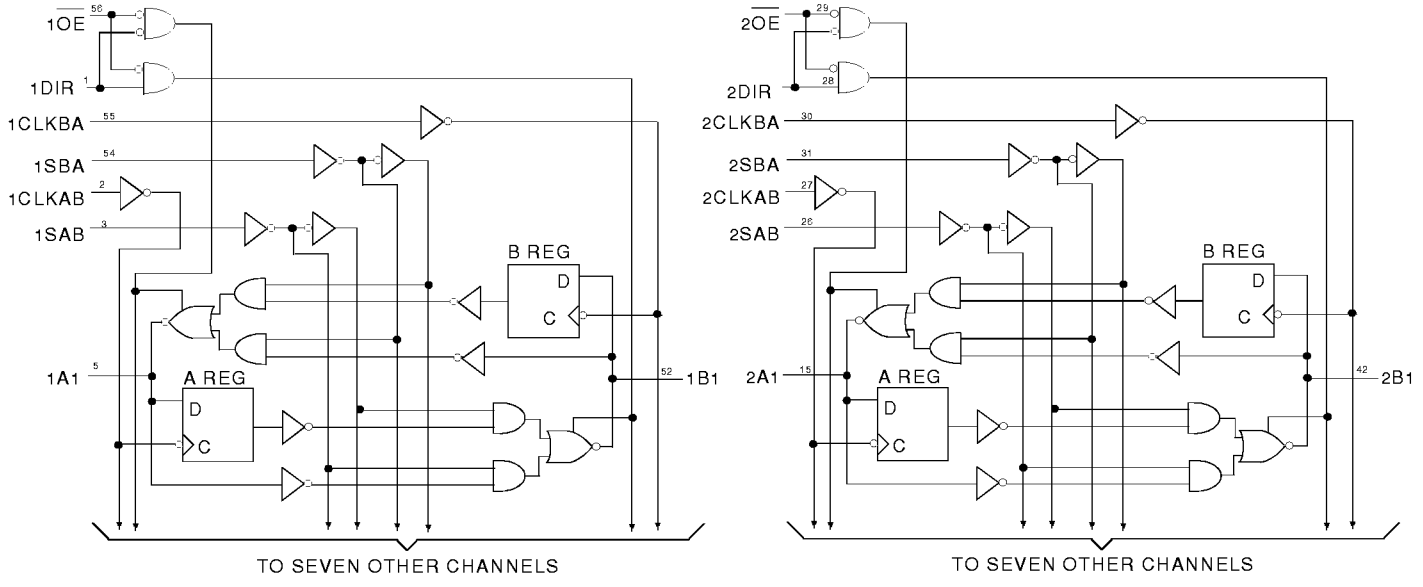
The LVCH162646A 16-bit transceiver/register is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type transceivers with 3-state D-type registers. The controls circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (DIR), over-riding Output Enable control ($\overline{OE}$) and Select lines (SAB and SBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the low-to-high transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

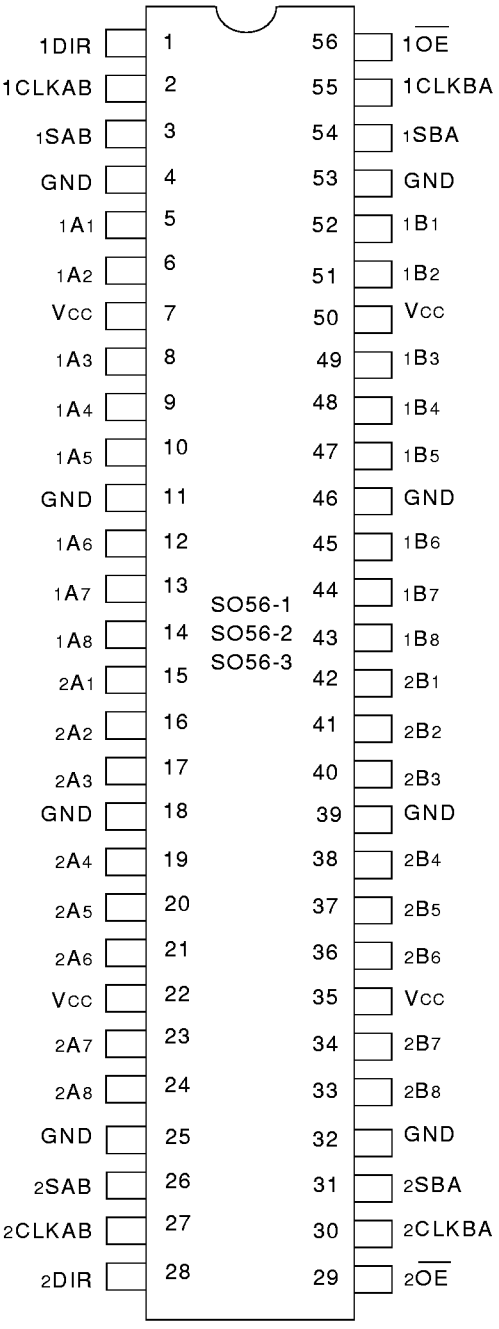
The LVCH162646A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive ±12mA at the designated threshold levels.

The LVCH162646A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/TVSOP TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	– 50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

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NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs(1) Data Register B Outputs
xBx	Data Register B Inputs(1) Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xDIR	Direction Control Inputs

NOTE:
1. These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (1)

Inputs						Data I/O(2)		
$x\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	Operation or Function
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified (2)
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified (2)
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to bus

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = Low-to-High Transition
2. The data-output functions may be enabled or disabled by various signals at $\overline{OE}$ or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
I_{CCZ}			3.6 ≤ V_{IN} ≤ 5.5V(2)	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V other inputs at V_{CC} or GND		—	—	500	µA

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NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

BUS HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	—	—	—	µA
I_{BHL}			V_I = 0.7V	—	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

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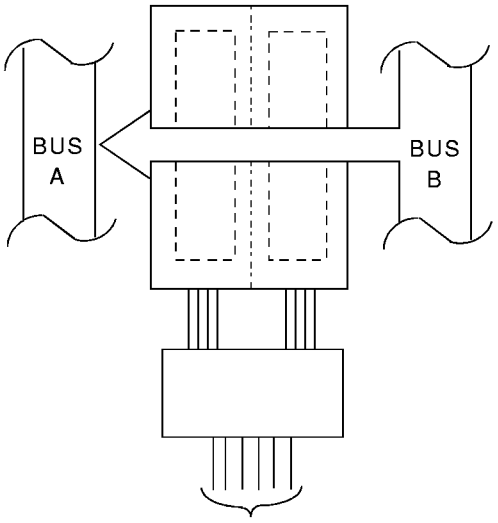
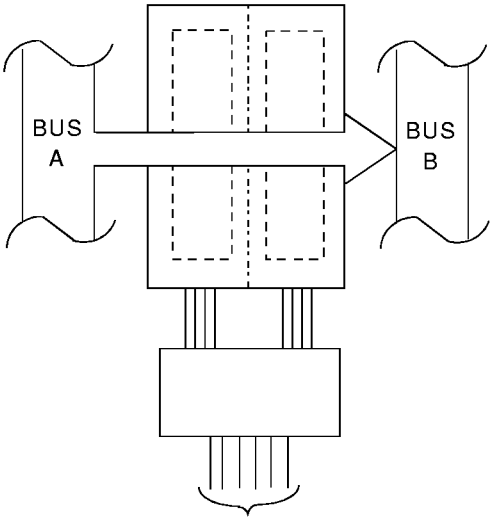
NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.



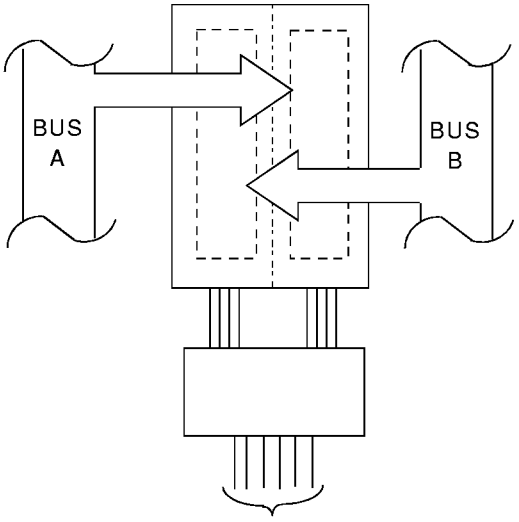
xDIR	$\overline{xOE}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO A



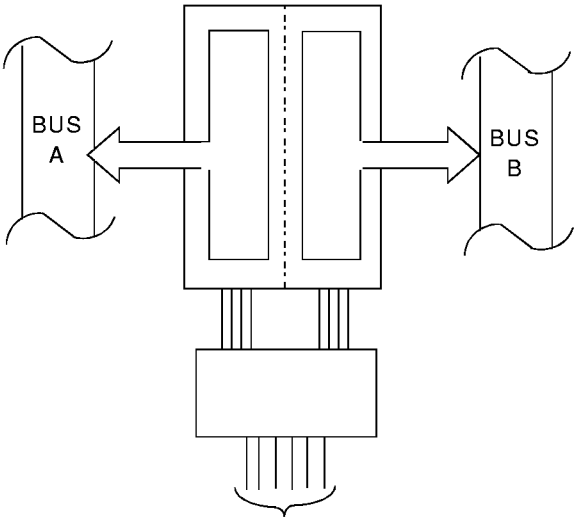
xDIR	$\overline{xOE}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

REAL-TIME TRANSFER
BUS A TO B



xDIR	$\overline{xOE}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



xDIR[(1)]	$\overline{xOE}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

TRANSFER STORED
DATA TO A AND/OR B

NOTE:
1. Cannot transfer data to A Bus and B Bus simultaneously..

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 4mA	1.9	—	
			I_{OH} = – 6mA	1.7	—	
		V_{CC} = 2.7V	I_{OH} = – 4mA	2.2	—	
			I_{OH} = – 8mA	2	—	
		V_{CC} = 3.0V	I_{OH} = – 6mA	2.4	—	
			I_{OH} = – 12mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 6mA	—	0.55	
		V_{CC} = 2.7V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 8mA	—	0.6	
		V_{CC} = 3.0V	I_{OL} = 6mA	—	0.55	
			I_{OL} = 12mA	—	0.8	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per transceiver Outputs enabled	C_L = 0pF, f = 10Mhz	—	pF
C_{PD}	Power Dissipation Capacitance per transceiver Outputs disabled		—	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx	2	6.3	2	5.3	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to xAx or xBx	2	7.3	2	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to xAx or xBx	2	7.3	2	6.3	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xAx or xBx	2	8.5	2	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to xAx or xBx	2	8.5	2	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xAx or xBx	2	7	2	6	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to xAx or xBx	2	7	2	6	ns
t_{SU}	Set-up Time HIGH or LOW Before CLKAB↑ or CLKBA↑	2.5	—	2.5	—	ns
t_H	Hold Time HIGH or LOW After CLKAB↑ or CLKBA↑	1.5	—	1.5	—	ns
tw	Clock Pulse Width HIGH or LOW	3	—	3	—	ns
$t_{SK}(o)$	Output Skew(2)	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$ = 3.3V ±0.3V	$V_{CC}^{(1)}$ = 2.7V	$V_{CC}^{(2)}$ = 2.5V ±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	V_{CC} / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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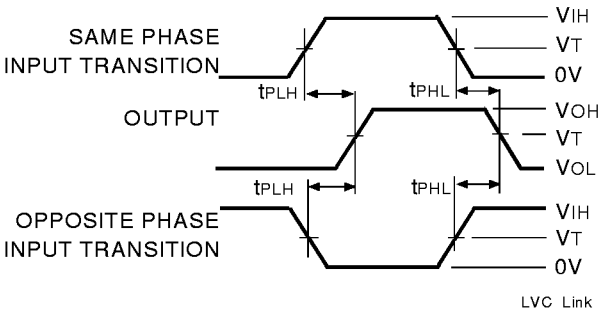
PROPAGATION DELAY



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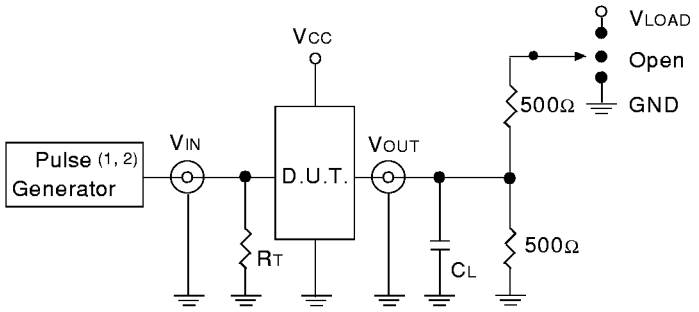
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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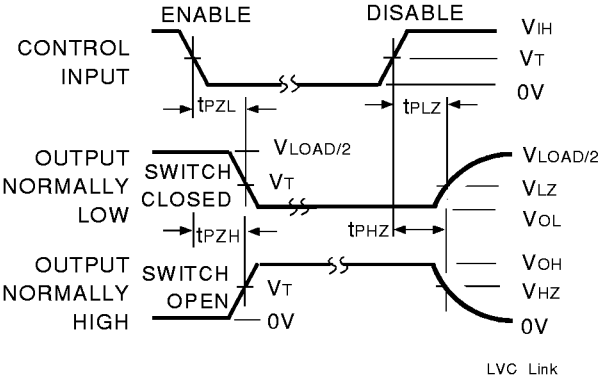
ENABLE AND DISABLE TIMES



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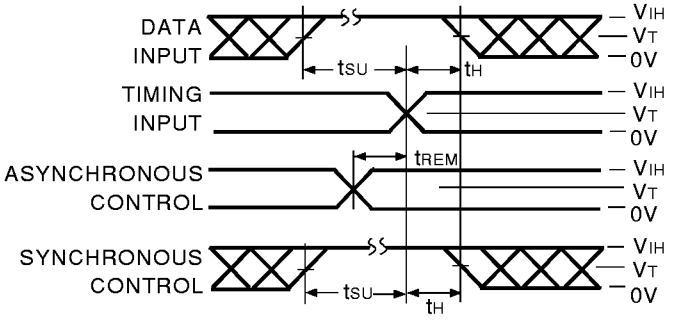
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD AND RELEASE TIMES



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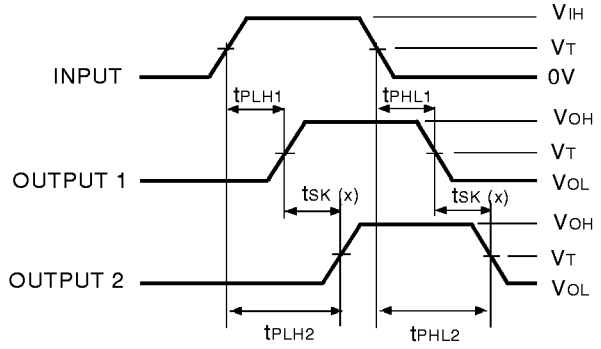
OUTPUT SKEW - t_{SK} (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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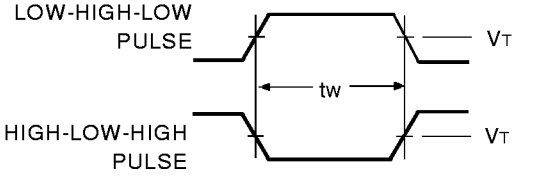
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PULSE WIDTH



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ORDERING INFORMATION