

## CMOS Analog Switches

### DESCRIPTION

The DG300B to DG303B family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

Designed on the Vishay Siliconix PLUS-40 CMOS process, these switches are latch-up proof, and are designed to block up to 30 V peak-to-peak when off. An epitaxial layer prevents latchup.

In the on condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their low on-resistance.

Featuring low power consumption (3.5 mW typ.) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are CMOS and quasi TTL compatible. Single supply operation is allowed by connecting the V- rail to 0 V.

### FEATURES

- Analog signal range:  $\pm 15\text{ V}$
- Fast switching -  $t_{ON}$ : 150 ns
- Low on-resistance -  $R_{DS(on)}$ : 30  $\Omega$
- Single supply operation
- Latch-up proof
- CMOS compatible

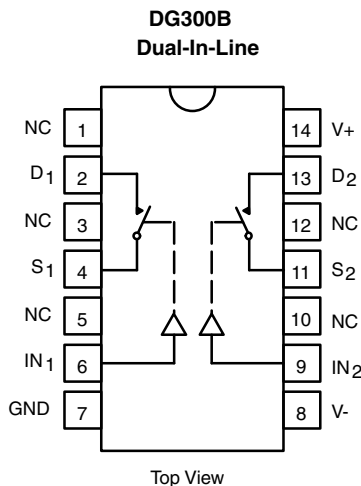
### BENEFITS

- Full rail-to-rail analog signal range
- Low signal error
- Low power dissipation

### APPLICATIONS

- Low level switching circuits
- Programmable gain amplifiers
- Portable and battery powered systems
- High-Rel systems

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

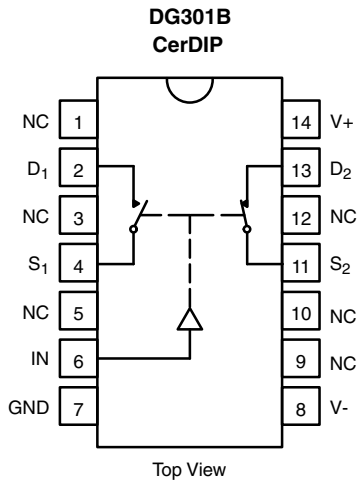


TRUTH TABLE	
LOGIC	SWITCH
0	Off
1	On

#### Notes

- Logic "0"  $\leq 0.8\text{ V}$
- Logic "1"  $\geq 4\text{ V}$

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

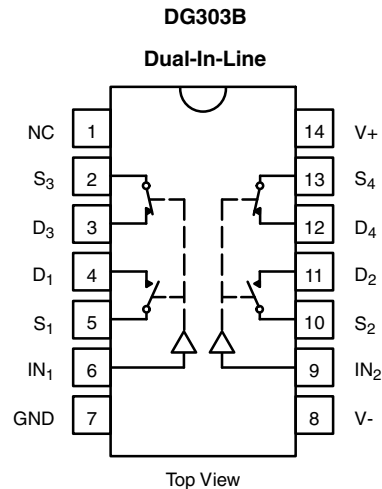
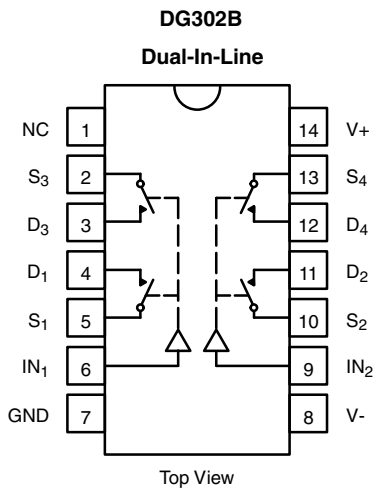


TRUTH TABLE		
LOGIC	SW <sub>1</sub>	SW <sub>2</sub>
0	Off	On
1	On	Off

**Notes**

- Logic "0" ≤ 0.8 V
- Logic "1" ≥ 4 V

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE	
LOGIC	SWITCH
0	Off
1	On

**Notes**

- Logic "0" ≤ 0.8 V
- Logic "1" ≥ 4 V

TRUTH TABLE		
LOGIC	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	Off	On
1	On	Off

**Notes**

- Logic "0" ≤ 0.8 V
- Logic "1" ≥ 4 V

ORDERING INFORMATION						
PART	CONFIGURATION	TEMP. RANGE	PACKAGE	ORDERING PART	GENERIC	DSCC NUMBER
DG300B	SPST x 2, NO	- 55 °C to 125 °C	14-pin CerDIP	DG300BAK/883	DG300BAK/883	(Vishay qualified, DSCC approval in progress)
DG301B	SPDT x 1			DG301BAK/883	DG301BAK/883	(Vishay qualified, DSCC approval in progress)
DG302B	DPST x 2, NO			DG302BAK/883	DG302BAK/883	(Vishay qualified, DSCC approval in progress)
DG303B	SPDT x 2			DG303BAK/883	DG303BAK/883	(Vishay qualified, DSCC approval in progress)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Voltages Referenced to V-	V+	44	V	
	GND	25		
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first		
Current (any terminal)		30	mA	
Continuous current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100		
Storage temperature		- 65 to 150	°C	
Power dissipation (package) <sup>b</sup>	14-pin CerDIP <sup>c</sup>	825	mW	

**Notes**

- a. Signals on S<sub>X</sub>, D<sub>X</sub> or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 11 mW/°C above 25 °C.

**SCHEMATIC DIAGRAM** (Typical Channel)

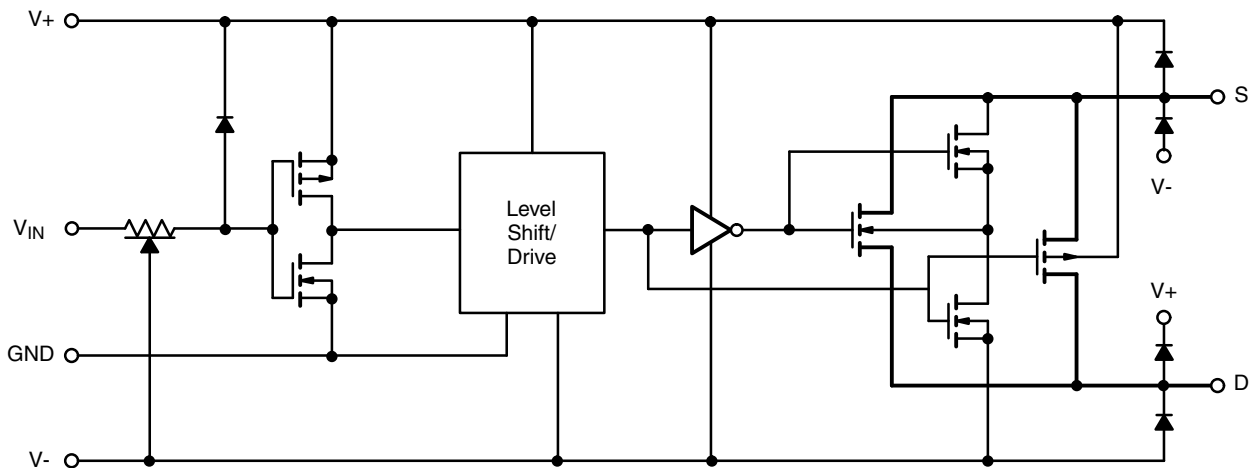


Fig. 1



SPECIFICATIONS <sup>a</sup>							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 0.8\text{ V}, V_{IN} = 4\text{ V}^f$	TEMP. <sup>b</sup>	LIMITS - 55 °C to 125 °C			UNIT
				MIN. <sup>d</sup>	TYP. <sup>c</sup>	MAX. <sup>d</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full	- 15		15	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_D = \pm 10\text{ V}, I_S = -10\text{ mA}$	Room		30	50	$\Omega$
			Full			75	
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}, V_D = \pm 14\text{ V}$	Room	- 1	$\pm 0.1$	1	nA
			Hot	- 100		100	
Drain Off Leakage Current	$I_{D(off)}$		Room	- 1	$\pm 0.1$	1	
			Hot	- 100		100	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 14\text{ V}$	Room	- 1	$\pm 0.1$	1	
			Hot	- 100		100	
<b>Digital Control</b>							
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room	- 1	- 0.001		$\mu\text{A}$
			Full	- 1			
		$V_{IN} = 15\text{ V}$	Room		0.001	1	
			Full			1	
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Room	- 1	- 0.001		
			Full	1			
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	see figure 2	Room		150	225	ns
Turn-Off Time	$t_{OFF}$		Room		130	190	
Break-Before-Make Time	$t_{OPEN}$	DG301B, DG303B only, figure 3	Room		50		
Charge Injection	Q	$C_L = 1\text{ nF}, R_{gen} = 0\ \Omega, V_{gen} = 0\text{ V}$ , figure 4	Room		8		pC
Source Off Capacitance	$C_{S(off)}$	$V_S, V_D = 0\text{ V}, f = 1\text{ MHz}$	Room		14		pF
Drain Off Capacitance	$C_{D(off)}$		Room		14		
Drain On Capacitance	$C_{D(on)}$		Room		40		
			Room		6		
Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$	$V_{IN} = 0\text{ V}$	Room		6	
			$V_{IN} = 15\text{ V}$	Room		7	
Off Isolation	OIRR	$V_{IN} = 0\text{ V}, R_L = 1\text{ k}\Omega$ $V_S = 1\text{ V}_{RMS}, f = 500\text{ kHz}$	Room		62		dB
Crosstalk	$X_{TALK}$		Room		74		
<b>Power Supplies</b>							
Positive Supply Current	I+	$V_{IN} = 4\text{ V}$ (one input) all others = 0 V	Room		0.23	1	mA
			Full				
Negative Supply Current	I-		Room	- 100	- 0.001		$\mu\text{A}$
			Full	- 100			
Positive Supply Current	I+	$V_{IN} = 0.8\text{ V}$ (all inputs)	Room		0.001	100	
			Full			100	
Negative Supply Current	I-		Room	- 100	- 0.001		
			Full	100			

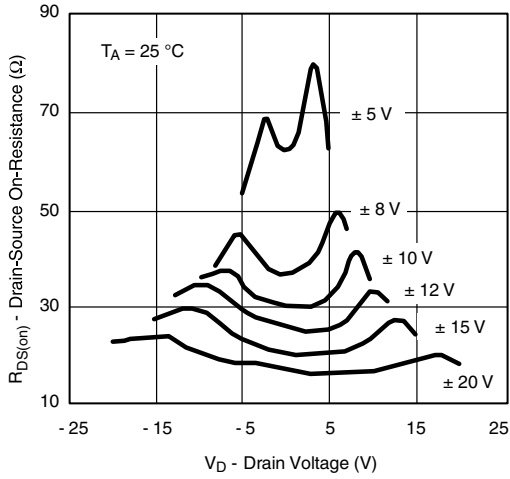
**Notes**

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

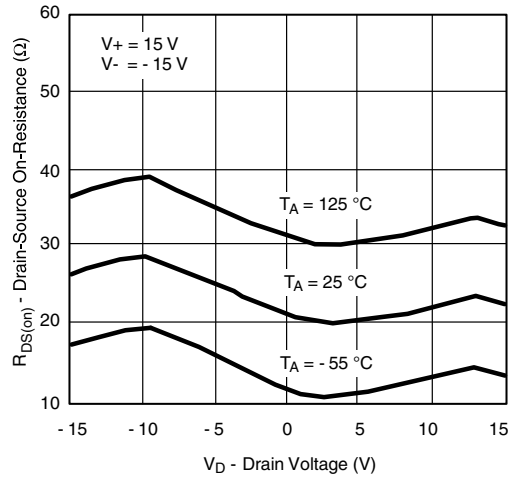
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



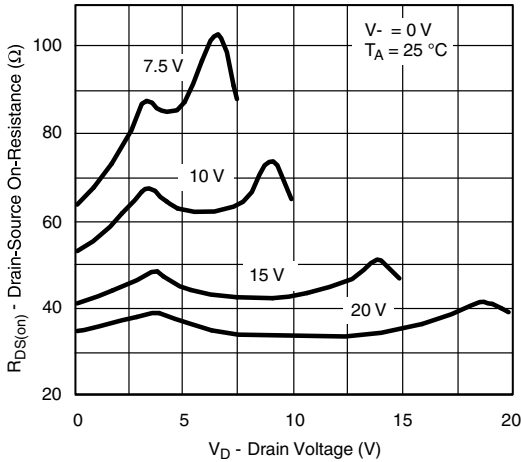
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



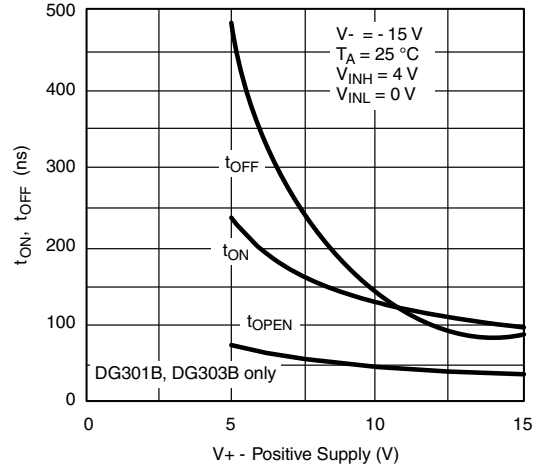
**R<sub>DS(on)</sub> vs. V<sub>D</sub> and Power Supply**



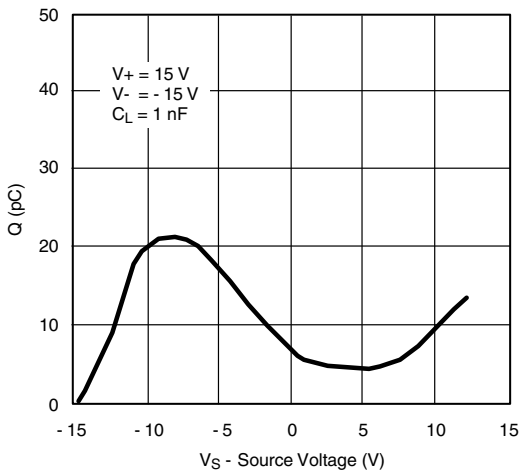
**R<sub>DS(on)</sub> vs. V<sub>D</sub> and Temperature**



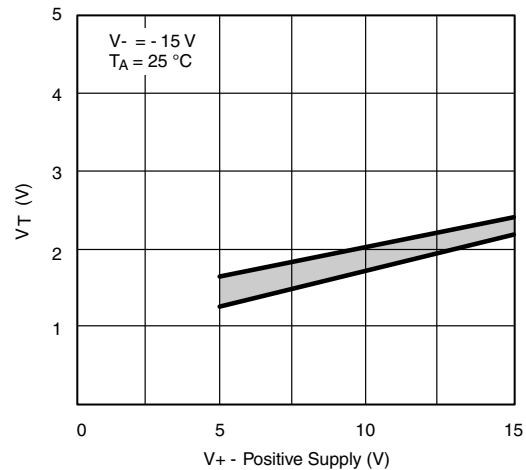
**R<sub>DS(ON)</sub> vs. V<sub>D</sub> and Power Supply Voltage**



**Switching Time and Break-Before-Make Time vs. Positive Supply Voltage**



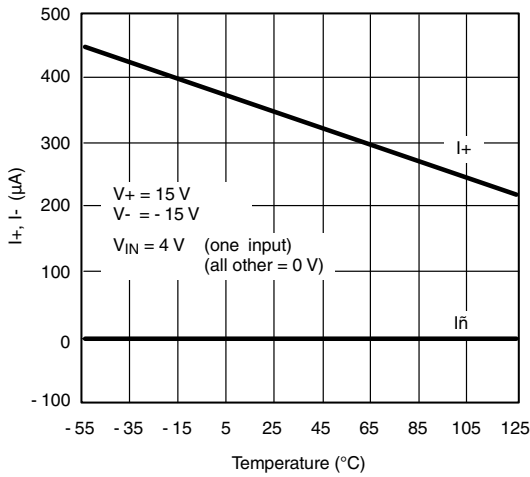
**Charge Injection vs. Analog Voltage**



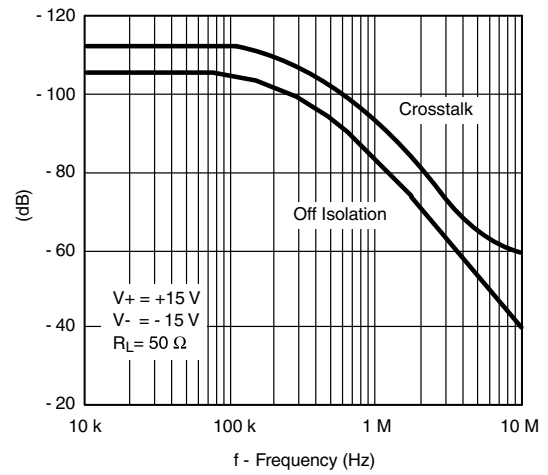
**Input Switching Threshold vs. Positive Supply Voltage**



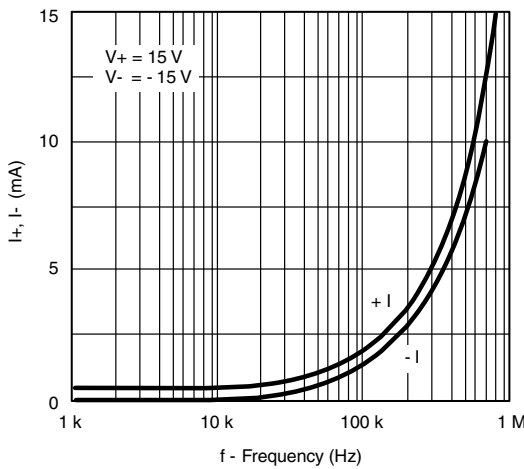
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



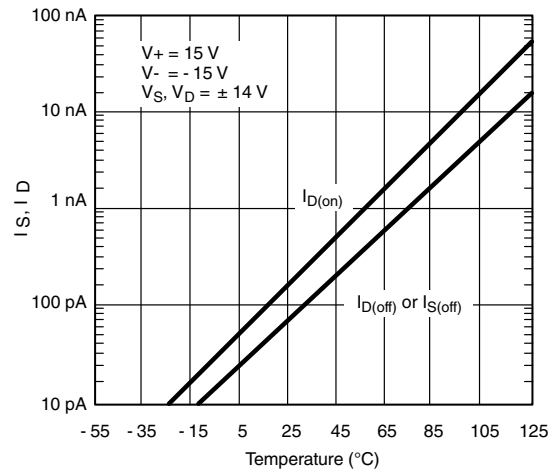
**Supply Current vs. Temperature**



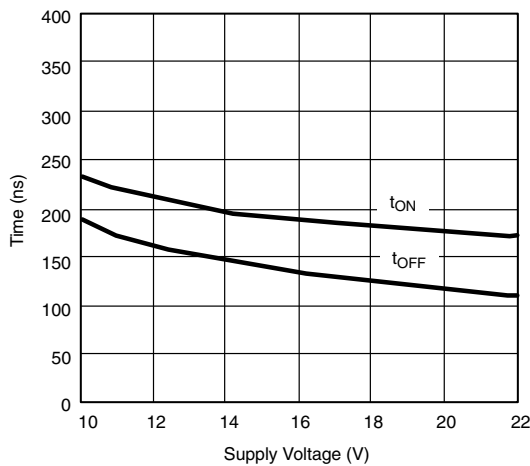
**Off Isolation and Crosstalk vs. Frequency**



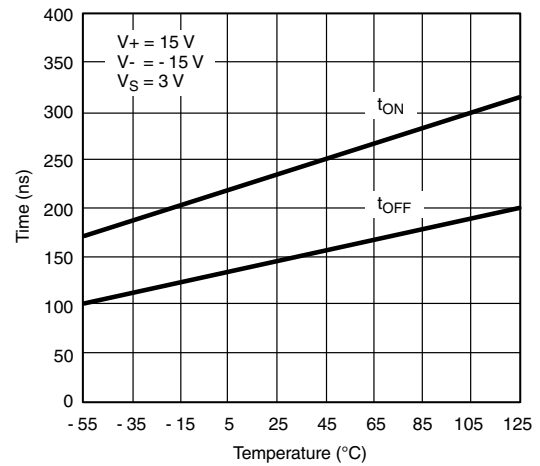
**Supply Current vs. Switching Frequency**



**Leakage vs. Temperature**



**Switching Time vs. Power Supply Voltage**



**Switching Time vs. Temperature**

## TEST CIRCUITS

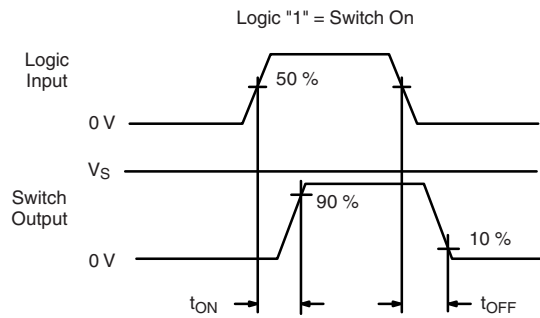
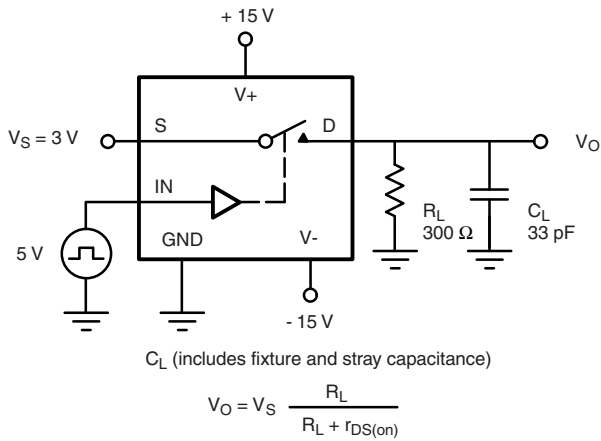


Fig. 2 - Switching Time

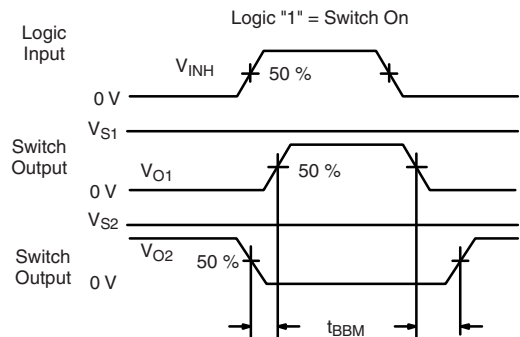
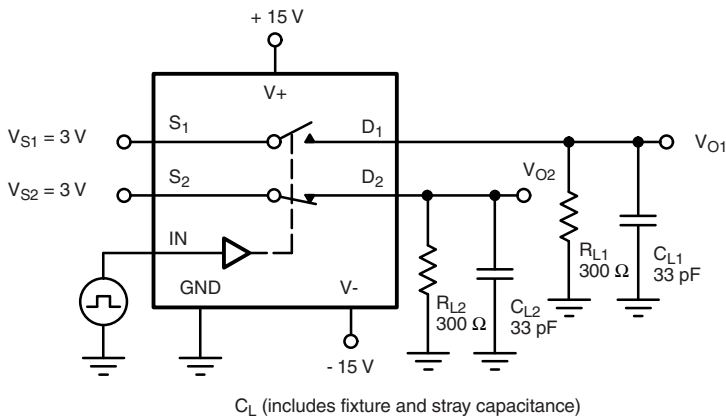


Fig. 3 - Break-Before-Make SPDT (DG301B, DG303B)

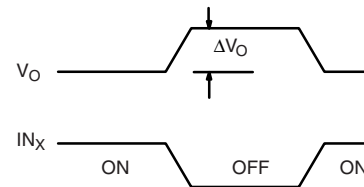
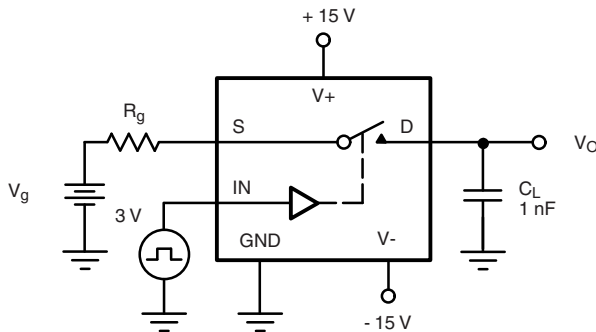


Fig. 4 - Charge Injection

## APPLICATION HINTS<sup>a</sup>

V <sub>+</sub> Positive Supply Voltage (V)	V <sub>-</sub> Negative Supply Voltage (V)	GND Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min.)</sub> /V <sub>INL(max.)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	- 15	0	4/0.8	- 15 to 15
20	- 20	0	4/0.8	- 20 to 20
15	0	0	4/0.8	0 to 15

### Note

a. Application hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

## APPLICATIONS

The DG300B series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are:

1. Increased R<sub>DS(on)</sub>.
2. Slower switching speed. The analog voltage should not go above or below the supply voltages which in single operation are V<sub>+</sub> and 0 V. (see Input Switching Threshold vs. Positive Supply Voltage curve.)

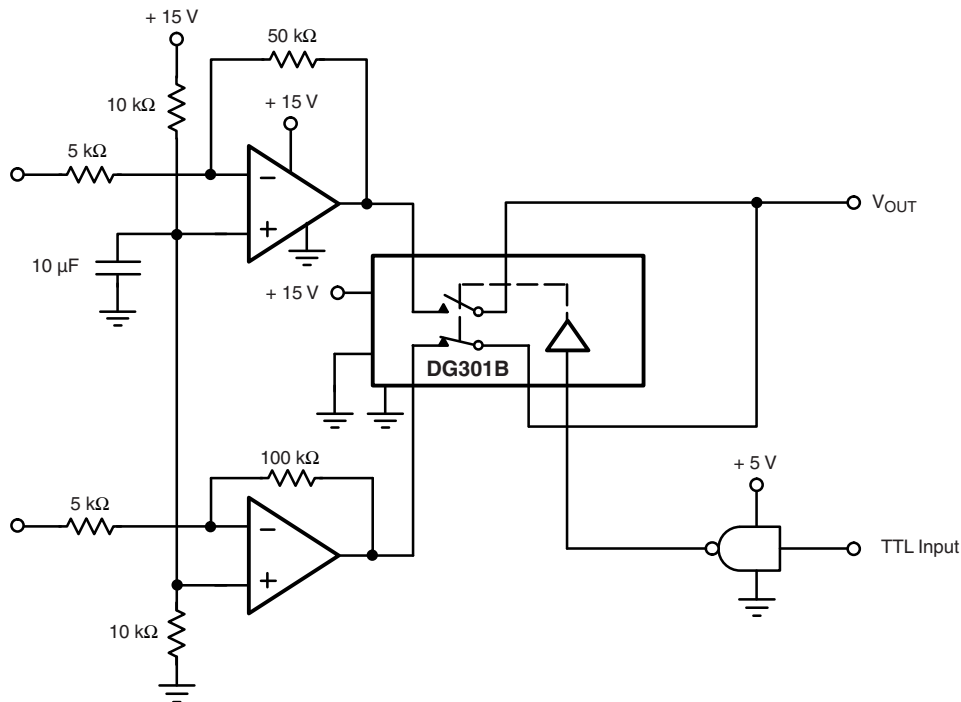
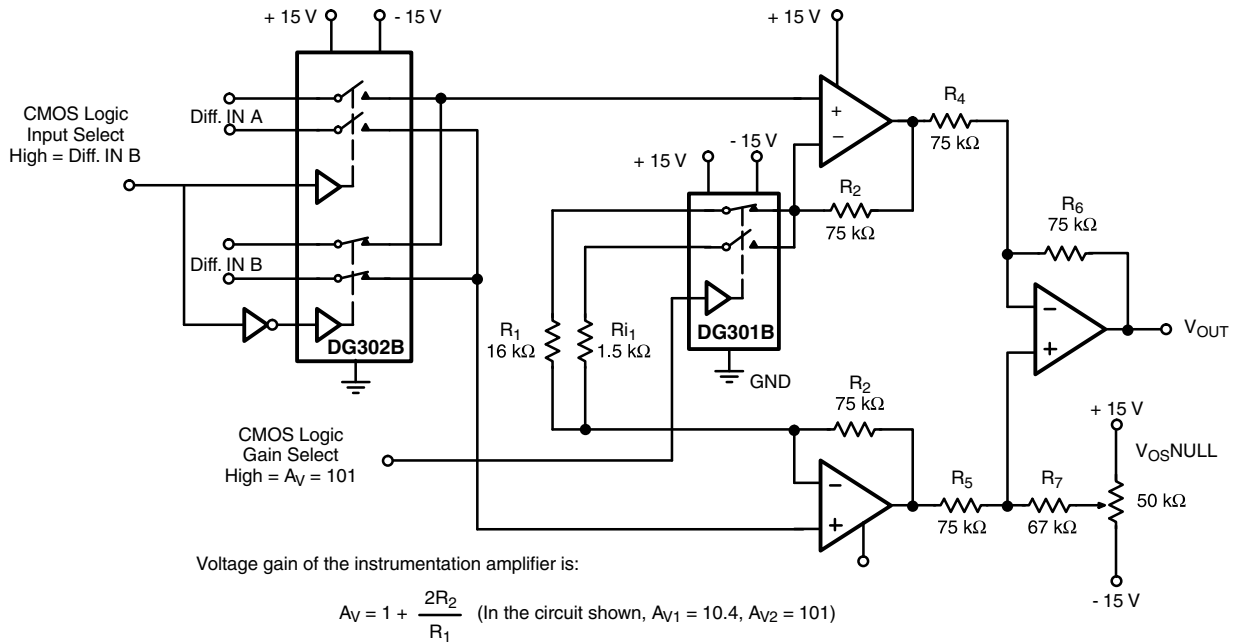


Fig. 5 - Single Supply Op. Amp. Switching



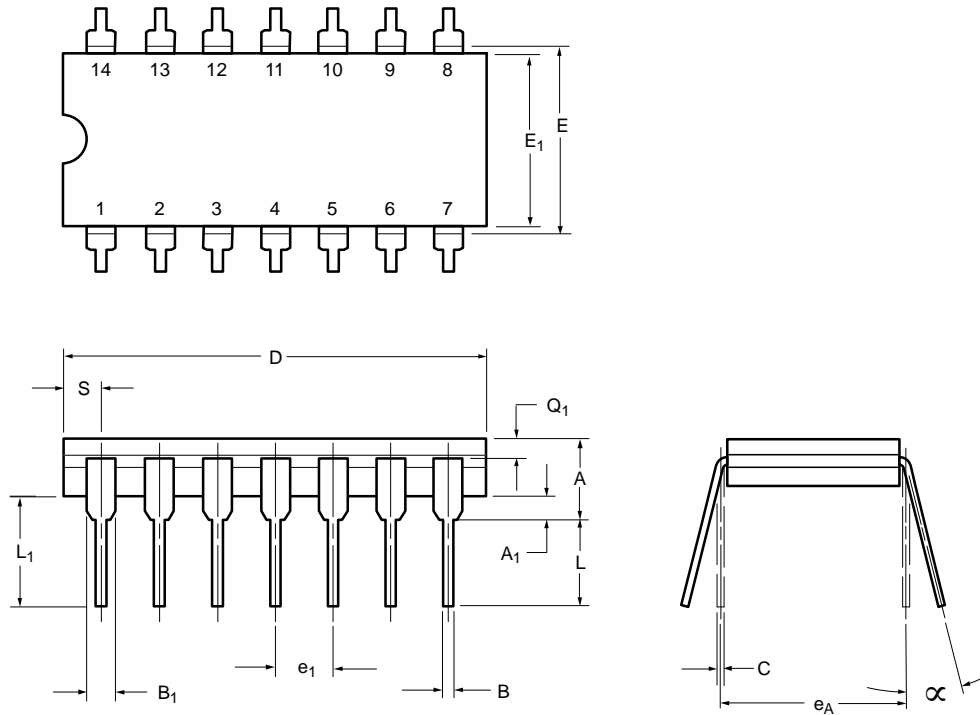
## APPLICATIONS



**Fig. 6 - Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?67936](http://www.vishay.com/ppg?67936).

### CERDIP: 14-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	4.06	5.08	0.160	0.200
<b>A<sub>1</sub></b>	0.51	1.14	0.020	0.045
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	1.14	1.65	0.045	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	19.05	19.56	0.750	0.770
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	6.60	7.62	0.260	0.300
<b>e<sub>1</sub></b>	2.54 BSC		0.100 BSC	
<b>e<sub>A</sub></b>	7.62 BSC		0.300 BSC	
<b>L</b>	3.18	3.81	0.125	0.150
<b>L<sub>1</sub></b>	3.81	5.08	0.150	0.200
<b>Q<sub>1</sub></b>	1.27	2.16	0.050	0.085
<b>S</b>	1.65	2.41	0.065	0.095
<b>α</b>	0°	15°	0°	15°

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DWG: 5402



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