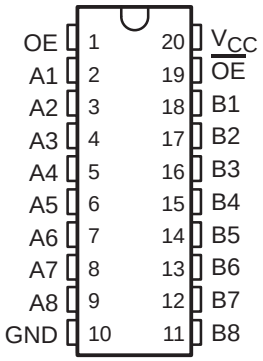
- **Standard ’245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Package Options Include Plastic Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3345 provides eight bits of high-speed TTL-compatible bus switching in a standard ’245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

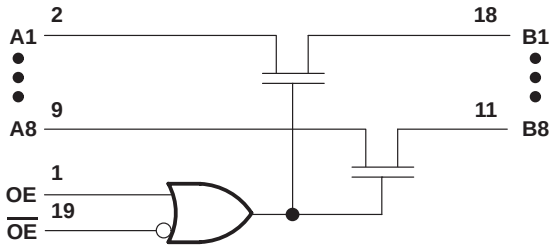
The device is organized as one 8-bit switch bank with dual output-enable ($\overline{OE}$ and OE) inputs. When $\overline{OE}$ is low or OE is high, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high and OE is low, the switch is open, and a high-impedance state exists between the two ports.

The SN74CBT3345 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C
DBQ package . . . . . 68°C
DGV package . . . . . 92°C
DW package . . . . . 58°C
PW package . . . . . 83°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	µA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC} or OE = GND			6		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

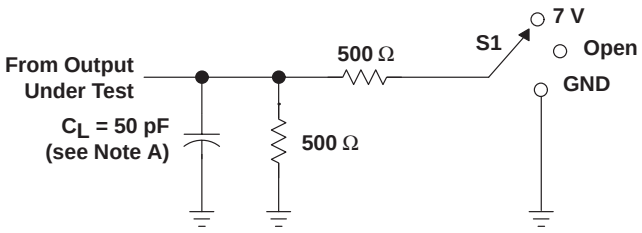
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$ or OE	A or B	1	9.1	ns
t_{dis}	$\overline{OE}$ or OE	A or B	1	8.7	ns

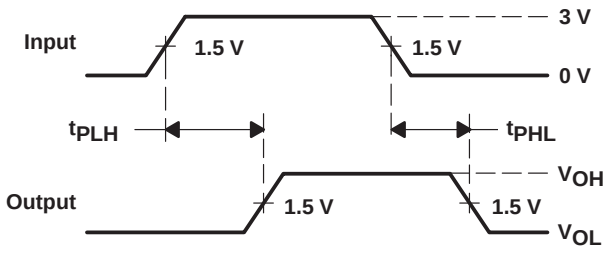
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

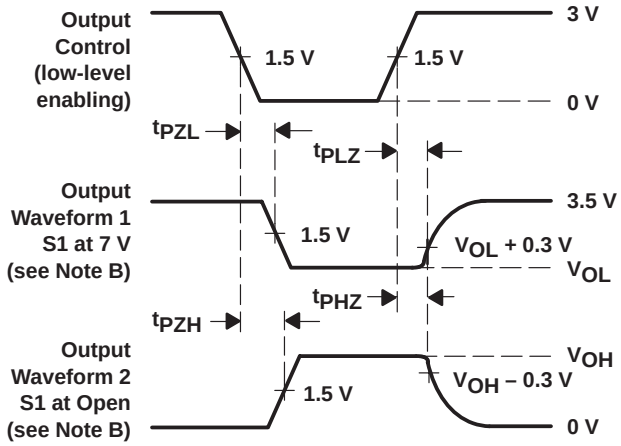


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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SN74CBT3345, 8-Bit FET Bus Switch

Device Status: Active

Parameter Name	SN74CBT3345
Voltage Nodes (V)	5
Vcc range (V)	4.0 to 5.5
No. of Bits	8
ron(max) (ohms)	7
tpd(max) (ns)	0.25

Description

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The SN74CBT3345 is characterized for operation from 0°C to 70°C.

Features

- Standard '245-Type Pinout
- 5- Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: scds027e.pdf (58 KB)
Full datasheet in Zipped PostScript: scds027e.psz (59 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
SN74CBT3345DBLE	DB	20	0 TO 70	OBSOLETE			
SN74CBT3345DBQR	DBQ	20	0 TO 70	ACTIVE	1.34	2500	Check stock or order
SN74CBT3345DBR	DB	20	0 TO 70	ACTIVE	1.17	2000	Check stock or order
SN74CBT3345DGVR	DGV	20	0 TO 70	ACTIVE	1.34	2000	Check stock or order
SN74CBT3345DW	DW	20	0 TO 70	ACTIVE	1.40	25	Check stock or order
SN74CBT3345DWR	DW	20	0 TO 70	ACTIVE	1.24	2000	Check stock or order
SN74CBT3345PWLE	PW	20	0 TO 70	OBSOLETE			
SN74CBT3345PWR	PW	20	0 TO 70	ACTIVE	1.17	2000	Check stock or order

Application Reports

View Application Reports for Digital Logic

- 5-V To 3.3-V Translation With The SN74CBTD3384 (SCDA003B - Updated: 03/01/1997)
- Flexible Voltage-Level Translation With CBT Family Devices (SCDA006 - Updated: 07/20/1999)
- Implications Of Slow Or Floating CMOS Inputs (SCBA004C - Updated: 02/01/1998)
- Low-Voltage Bus-Switch Technology And Applications (SCDA005 - Updated: 12/01/1997)
- Migration From 3.3-V To 2.5-V Power Supplies For Logic Devices (SCEA005 - Updated: 12/01/1997)
- SN74CBTS3384 Bus Switches Provide Fast Connection And Ensure Isolation (SCDA002A - Updated: 08/01/1996)
- TI Logic Solutions for Memory Interleaving With the Intel440BX Chipset (SCCA001 - Updated: 04/08/1999)
- Texas Instruments Crossbar Switches (SCDA001A - Updated: 06/01/1995)
- Texas Instruments Solution for Undershoot Protection for Bus Switches (SCDA007 - Updated: 04/13/2000)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)

Related Documents

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 284 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

Table Data Updated on: 8/31/2000