

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- *DOC™* (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Less Than 2-ns Maximum Propagation Delay at 2.5-V and 3.3-V V_{CC}
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Over-Voltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Feature Supports Partial Power-Down Mode Operation
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

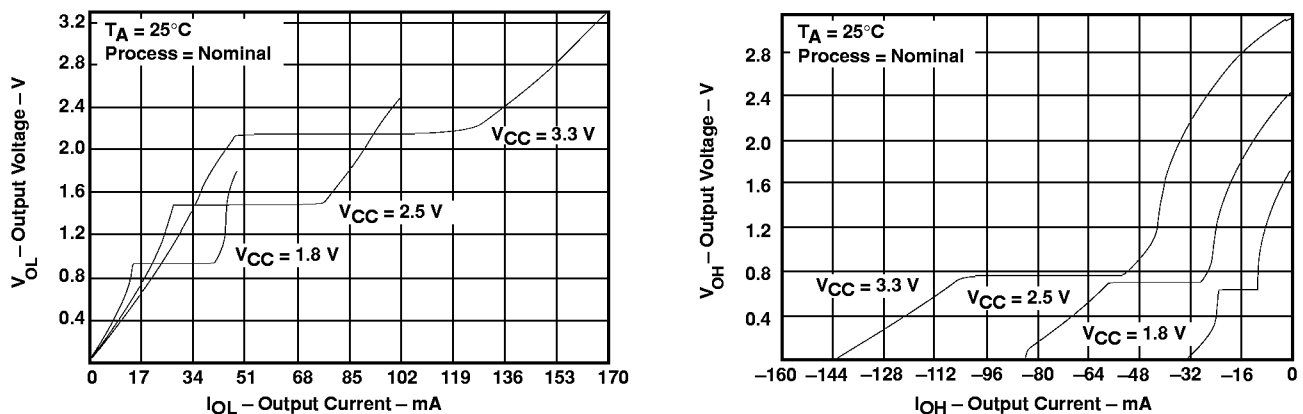


Figure 1. Output Voltage vs Output Current

This 16-bit (dual-octal) noninverting bus transceiver is operational at 1.5-V to 3.6-V V_{CC} , but designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74AVC16245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74AVC16245 is characterized for operation from -40°C to 85°C .



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 **TEXAS
INSTRUMENTS**

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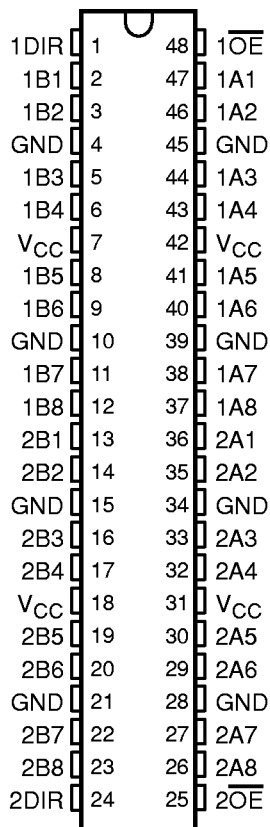
SN74AVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

DESIGN GOAL

SCES142D – JULY 1998 – REVISED DECEMBER 1998

terminal assignments

DGG OR DGV PACKAGE
(TOP VIEW)



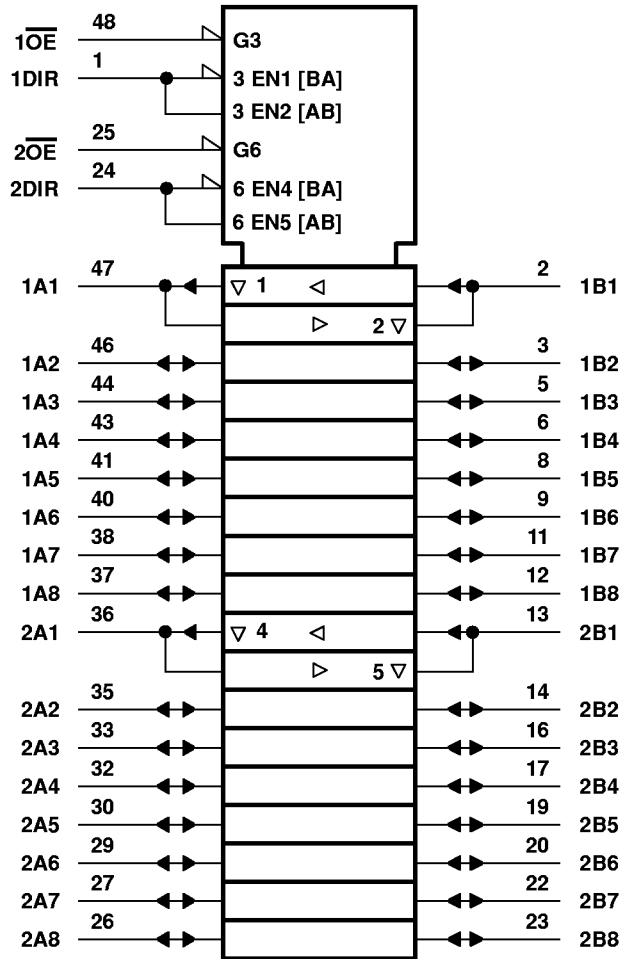
FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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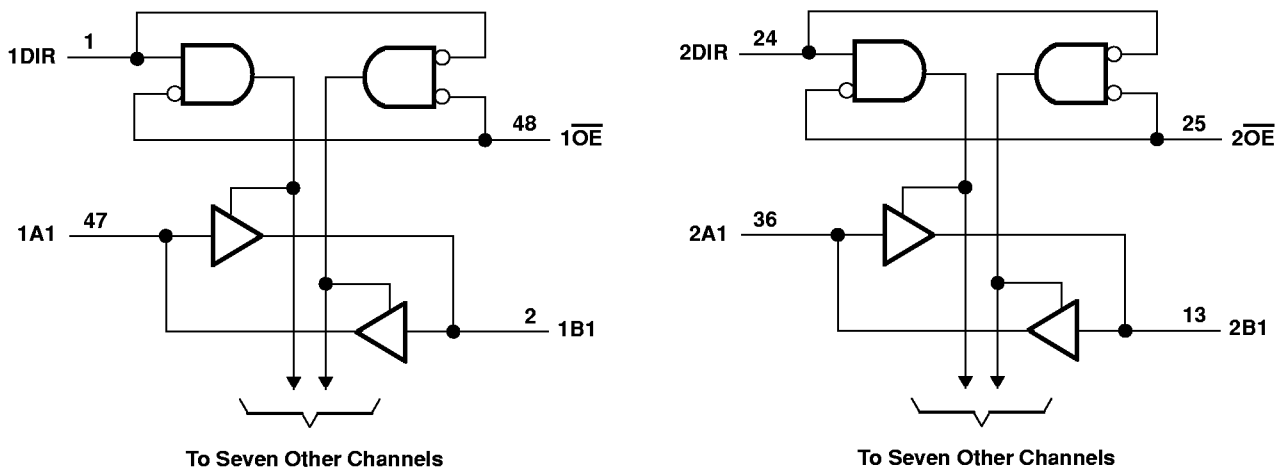


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN74AVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

DESIGN GOAL

SCES142D – JULY 1998 – REVISED DECEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DGV package	93°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.2		
V_{IH}	High-level input voltage	$V_{CC} = 1.2$ V	V_{CC}		V
		$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		
		$V_{CC} = 2.3$ V to 2.7 V	1.7		
		$V_{CC} = 3$ V to 3.6 V	2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.2$ V	GND		V
		$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$		
		$V_{CC} = 2.3$ V to 2.7 V	0.7		
		$V_{CC} = 3$ V to 3.6 V	0.8		
V_I	Input voltage	0	3.6	V	
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	V
I_{OHS}	Static high-level output current‡	$V_{CC} = 1.65$ V to 1.95 V	–4		mA
		$V_{CC} = 2.3$ V to 2.7 V	–8		
		$V_{CC} = 3$ V to 3.6 V	–12		
I_{OLS}	Static low-level output current‡	$V_{CC} = 1.65$ V to 1.95 V	4		mA
		$V_{CC} = 2.3$ V to 2.7 V	8		
		$V_{CC} = 3$ V to 3.6 V	12		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.65$ V to 3.6 V		5	ns/V
T_A	Operating free-air temperature	–40	85	°C	

‡ Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of ±24 mA at 2.5-V V_{CC} . See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to the TI application reports, **AVC Logic Family Technology and Applications**, literature number **SCEA006**, and **Dynamic Output Control (DOC™) Circuitry Technology and Applications**, literature number **SCEA009**.

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}		I _{OHS} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
		I _{OHS} = -4 mA, V _{IH} = 1.07 V	1.65 V	1.2			
		I _{OHS} = -8 mA, V _{IH} = 1.7 V	2.3 V	1.75			
		I _{OHS} = -12 mA, V _{IH} = 2 V	3 V	2.3			
V _{OL}		I _{OLS} = 100 μA	1.65 V to 3.6 V			0.2	V
		I _{OLS} = 4 mA, V _{IL} = 0.57 V	1.65 V			0.45	
		I _{OLS} = 8 mA, V _{IL} = 0.7 V	2.3 V			0.55	
		I _{OLS} = 12 mA, V _{IL} = 0.8 V	3 V			0.7	
I _I	Control inputs	V _I = V _{CC} or GND	3.6 V			±2.5	μA
I _{off}		V _I = 0 or 3.6 V	0			±10	μA
I _{OZ} ‡		V _O = V _{CC} or GND	3.6 V			±12.5	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
C _i	Control inputs	V _I = V _{CC} or GND	2.5 V	3			pF
			3.3 V	3			
C _{io}	A or B ports	V _O = V _{CC} or GND	2.5 V	10			pF
			3.3 V	10			

† Typical values are measured at T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.5 V	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A		1.3	3.2	0.9	1.9	0.8	1.7	ns
t _{en}	\overline{OE}	A or B		3	7.5	2.3	4.3	1.5	3.5	ns
t _{dis}	\overline{OE}	A or B		3.5	6.8	2.2	4.2	2.5	4.2	ns

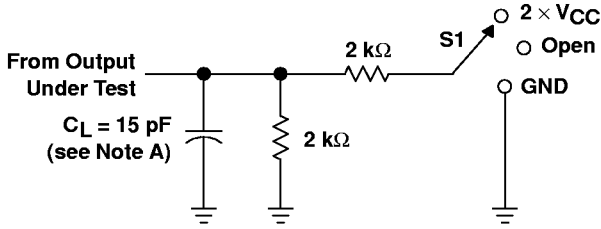
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	C _L = 0, f = 10 MHz	16	19	22	pF
			1	1	1	

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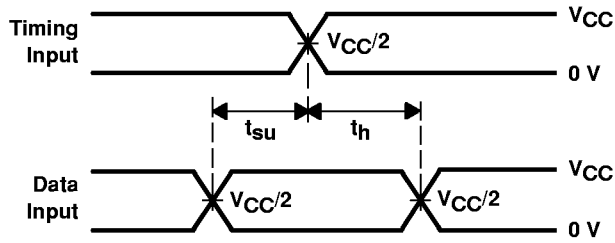
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.5\text{ V}$

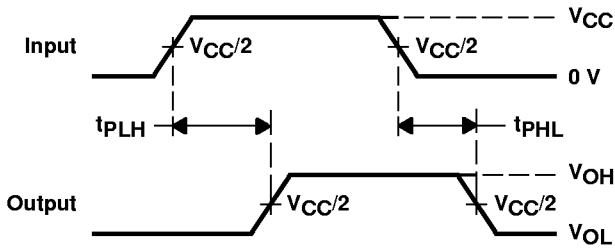


LOAD CIRCUIT

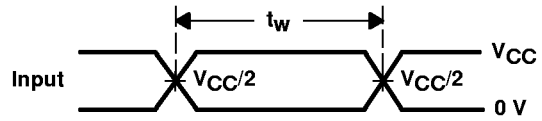
TEST	S1
t_{pd}	Open
t_{pLZ}/t_{pZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



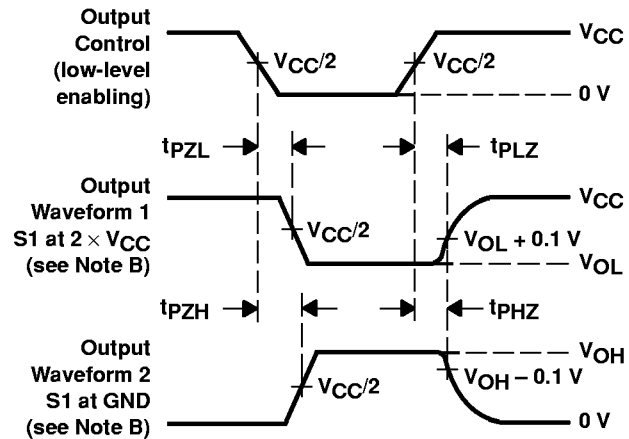
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

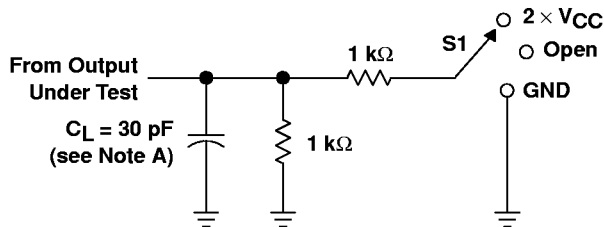
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - F. t_{pZL} and t_{pZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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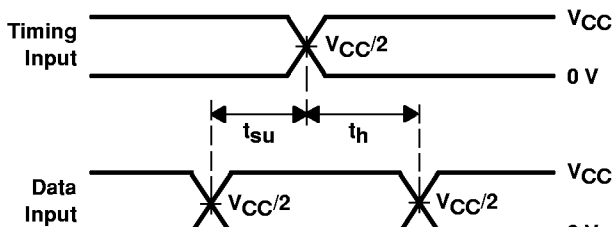
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

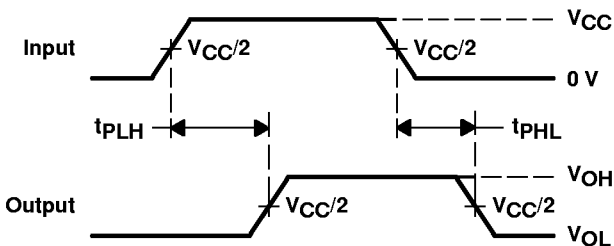


LOAD CIRCUIT

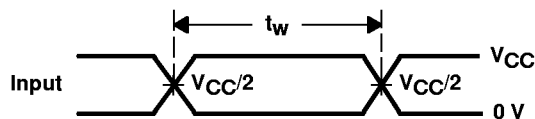
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



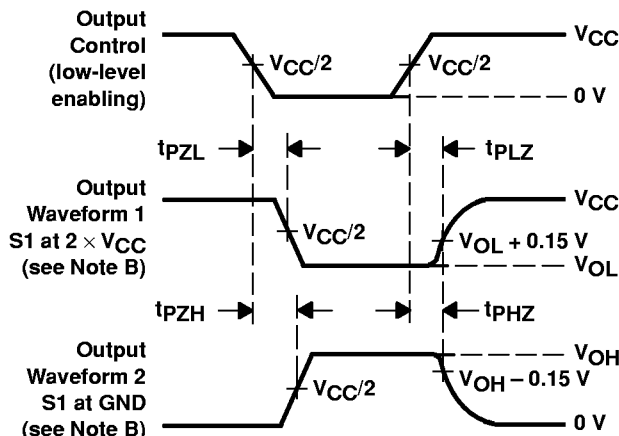
VOLTAGE WAVEFORMS
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PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

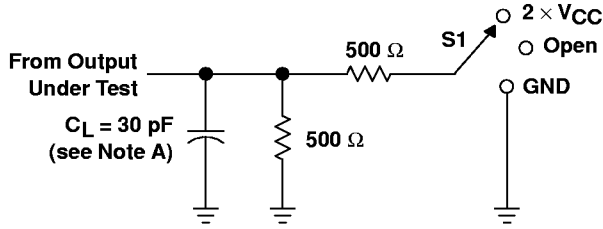
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 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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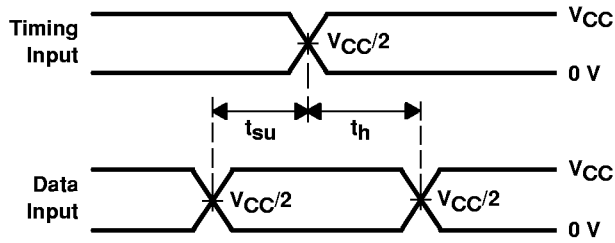
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

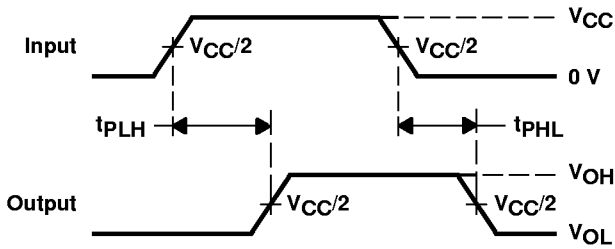


LOAD CIRCUIT

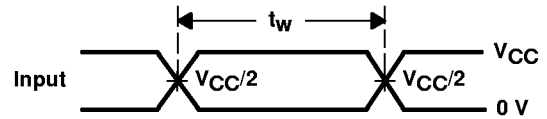
TEST	S1
t_{pd}	Open
t_{pLZ}/t_{pZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



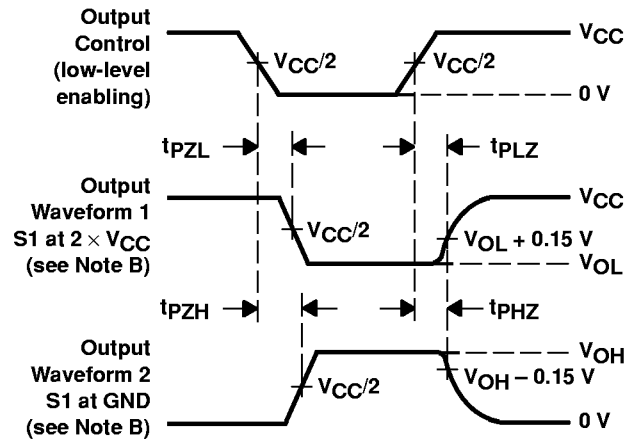
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
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**VOLTAGE WAVEFORMS
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**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

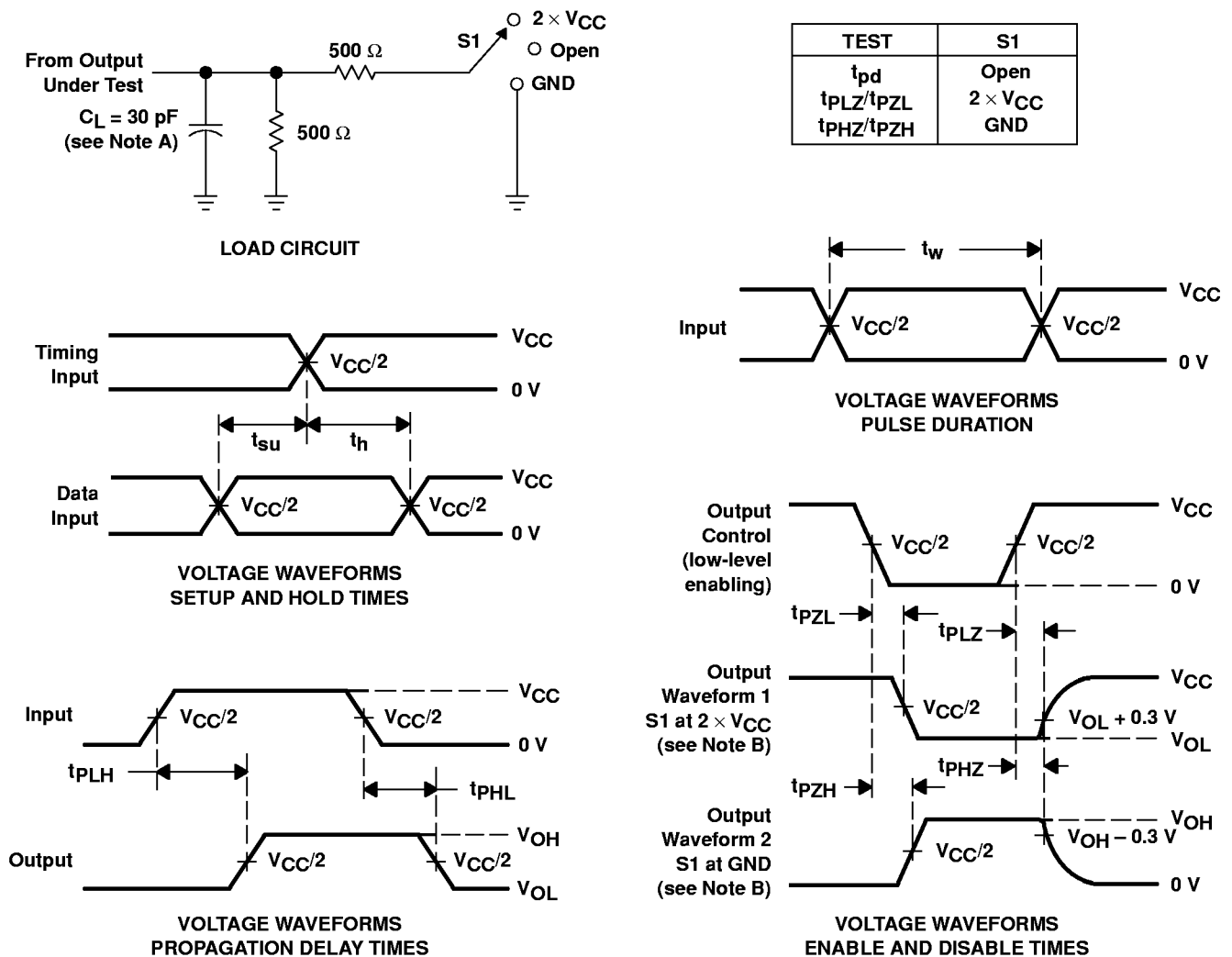
- NOTES:
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 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - F. t_{pZL} and t_{pZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
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 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

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