DATA SHEET

74LVT20
3.3V Dual 4-input NAND gate

Product specification

IC24 Data Handbook

1996 Aug 28

Philips
Semiconductors

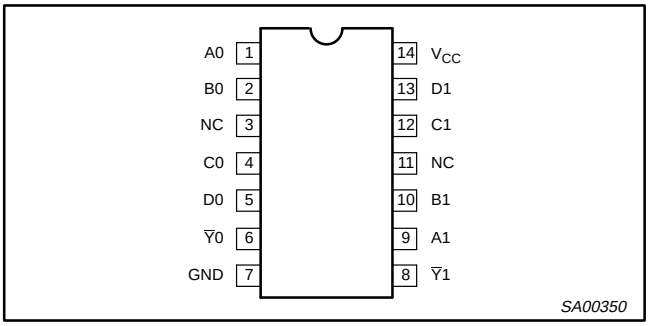
PHILIPS

3.3V Dual 4-input NAND gate 74LVT20

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn, Dn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 3.3V	3.4 3.2	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	0.5	mA

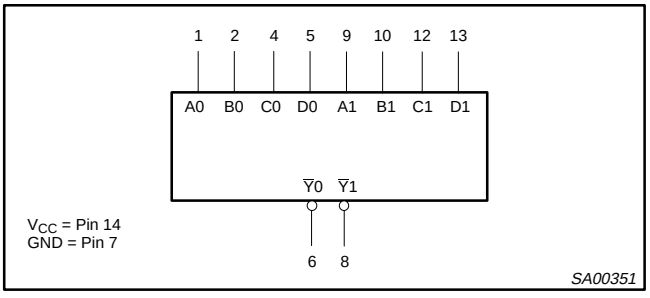
PIN CONFIGURATION



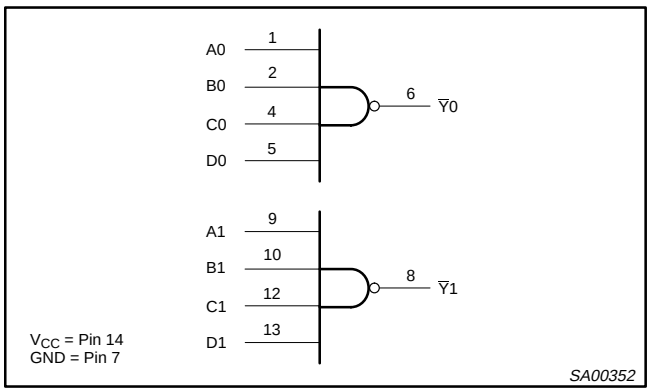
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An, Bn, Cn, Dn	Data inputs
6, 8	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

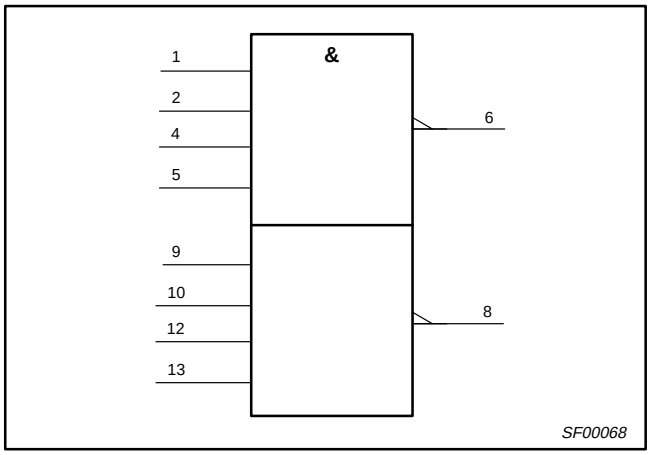
LOGIC SYMBOL



LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUT
Dna	Dnb	Dnc	Dnd	$\overline{Q}n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT20 D	74LVT20 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT20 DB	74LVT20 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT20 PW	74LVT20PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		48	
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		0.5	1.2	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

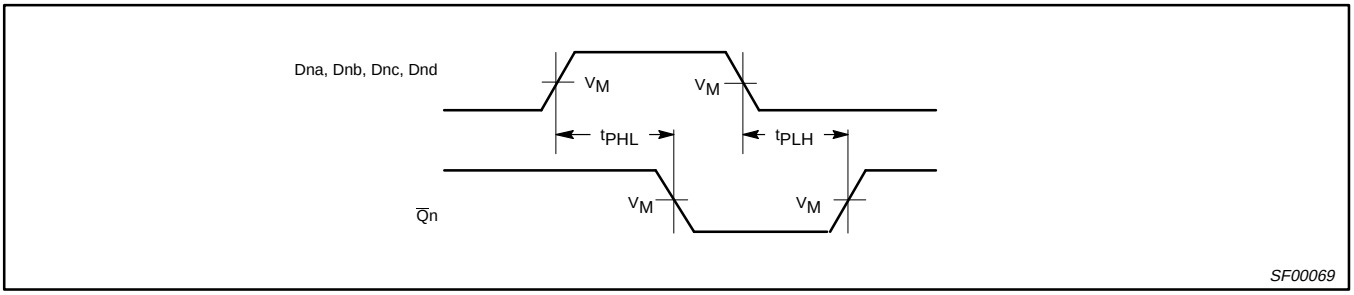
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn, Dn to $\overline{Y}$n	1	1.0 1.0	3.4 3.2	5.4 4.4	6.4 4.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

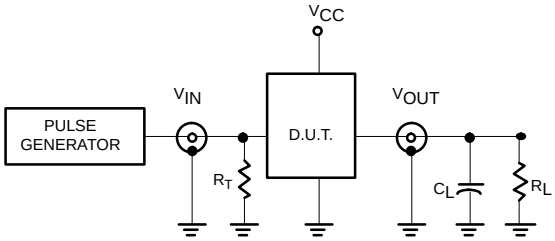
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

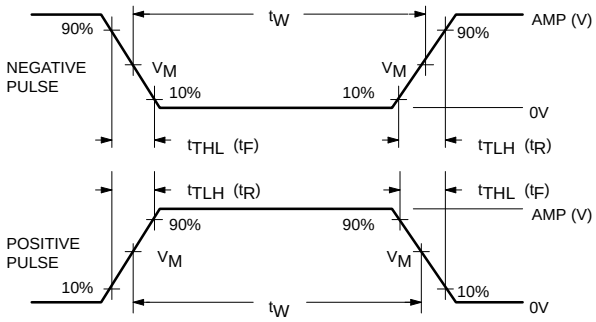


Waveform 1. Propagation Delay for Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

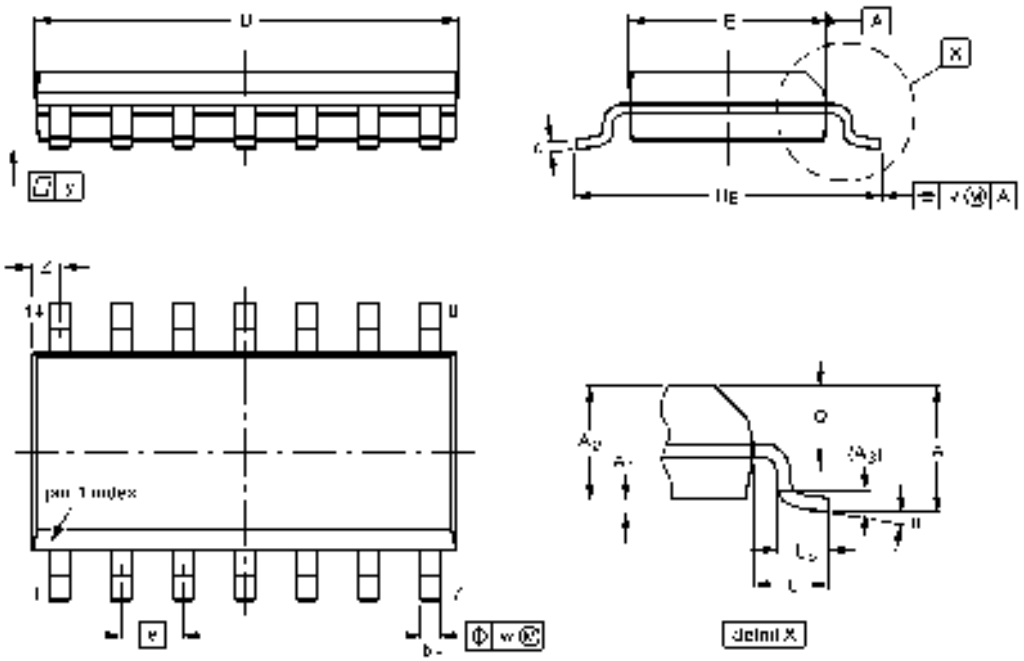
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

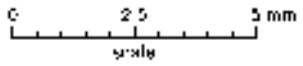
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00022

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

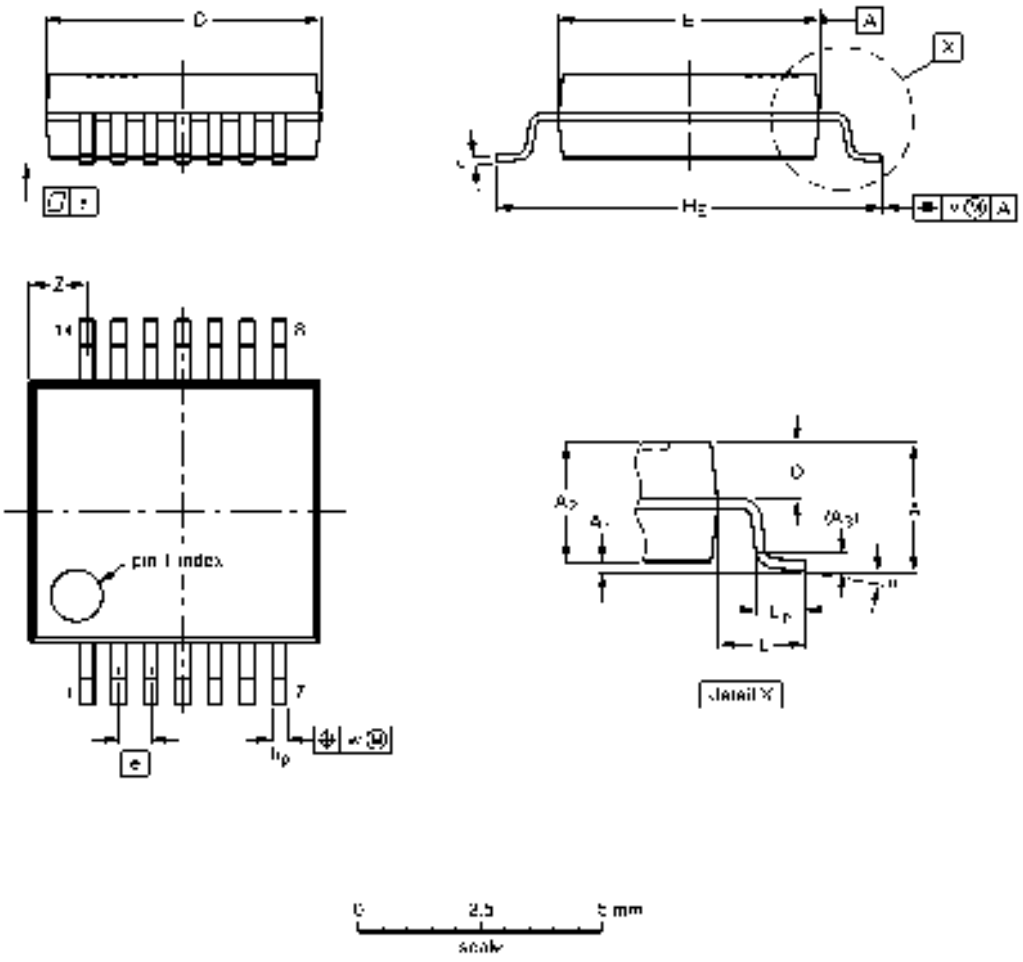
UNIT	A max.	A_1	A_2	A_3	b_p	c	D[1]	E[1]	e	H_E	L	L_p	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.029 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

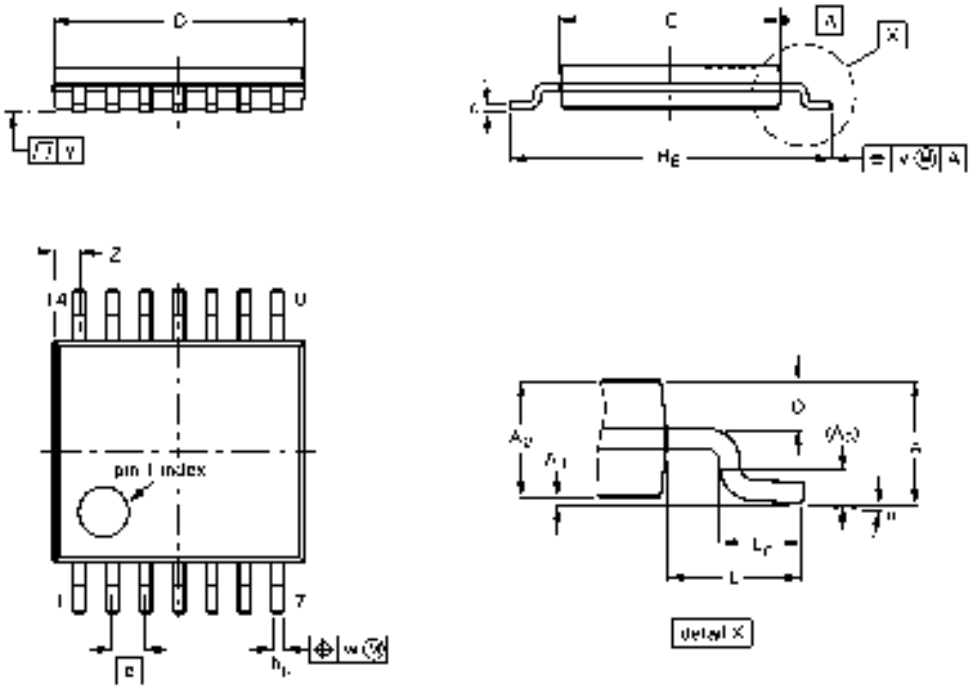
UNIT	A max.	A_1	A_2	A_3	b_p	c	D[1]	E[1]	e	H_E	L	L_p	Q	v	w	y	Z[1]	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

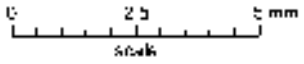
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm SOT402-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [1]	E [2]	e	H_E	L	L_p	Q	v	w	y	Z [1]	θ
mm	1.10	0.15 0.05	0.93 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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74LVT20; 3.3V Dual 4-input NAND gate

Information as of 2003-04-22

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Applications

- AN2022: The Behavior Of Integrated Bus Hold Circuits (date 01-Mar-96)
- AN203_2: Test Fixtures for High Speed Logic (date 02-Apr-98)
- AN2301: Simulation Support for Philips' Advanced BiCMOS Products
- AN243: LVT (Low Voltage Technology) and ALVT (Advanced LVT) (date 01-Jan-98)
- AN246: Transmission Lines and Terminations with Philips Advanced Logic Families

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74LVT20	3.3V Dual 4-input NAND gate	8/28/1996	Product specification	10	69	Download

Blockdiagram(s)

Block diagram of 74LVT20D

Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74LVT20D	SOT108-1 (SO14)	3.3V Dual 4-Input NAND Gate	4~6	Low	14	None	TTL	Medium
74LVT20DB	SOT337-1 (SSOP14)	3.3V Dual 4-Input NAND Gate	4~6	Low	14	None	TTL	Medium
74LVT20PW	SOT402-1 (TSSOP14)	3.3V Dual 4-Input NAND Gate	4~6	Low	14	None	TTL	Medium

Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing IC packing info	Package	Device status	Buy online
74LVT20D	74LVT20D	9352 092 00112	Standard Marking * Tube	SOT108-1 (SO14)	Full production	order this -
	74LVT20D-T	9352 092 00118	Standard Marking * Reel Pack, SMD, 13"	SOT108-1 (SO14)	Full production	order this -
74LVT20DB	74LVT20DB	9352 094 40112	Standard Marking * Tube	SOT337-1 (SSOP14)	Full production	order this -
	74LVT20DB-T	9352 094 40118	Standard Marking * Reel Pack, SMD, 13"	SOT337-1 (SSOP14)	Full production	order this -
74LVT20PW	74LVT20PW	9352 092 10112	Standard Marking * Tube	SOT402-1 (TSSOP14)	Full production	order this -
	74LVT20PW-T	9352 092 10118	Standard Marking * Reel Pack, SMD, 13"	SOT402-1 (TSSOP14)	Full production	order this -

Products in the above table are all in production. Some variants are discontinued; click here for information on these variants.

Similar products

74LVT20 links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

Support & tools

Innovative Low Voltage Logic Solutions(date 01-Aug-00)
Introduction to Advanced BiCMOS Logic Products(date 01-Mar-98)
Family specifications LVT, family characteristics(date 01-Mar-98)
Advanced BiCMOS features(date 01-Jan-98)

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  French Translate

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