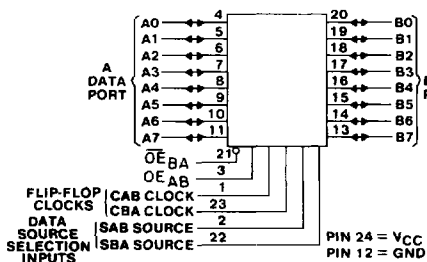


CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652



FUNCTIONAL DIAGRAM

92C5-42677

Octal-Bus Transceiver/Registers, 3-State

CD54/74AC/ACT651 - Inverting
CD54/74AC/ACT652 - Non-Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
5.3 ns @ $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50 pF$

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- ± 24 -mA output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

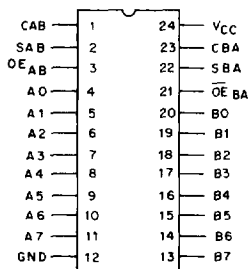
*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC651 and CD54/74AC652 and the CD54/74ACT651 and CD54/74ACT652 3-state, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC651 and CD54/74ACT651 have inverting outputs. The CD54/74AC652 and CD54/74ACT652 have non-inverting outputs. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE_{AB} and OE_{BA} are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and OE_{BA} . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD74AC/ACT651 and CD74AC/ACT652 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT651 and CD54AC/ACT652, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.



92C5-42678

TERMINAL ASSIGNMENT

CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION | |
|------------------|------------------|--------|--------|-----|-----|--------------|--------------|--|--|
| OE _{AB} | OE _{BA} | CAB | CBA | SAB | SBA | A0 THRU A7 | B0 THRU B7 | 651 | 652 |
| L | H | H or L | H or L | X | X | Input | Input | Isolation* | Isolation* |
| H | H | | | X | X | Input | Input | Store A and B Data | Store A and B Data |
| X | H | | H or L | X | X | Input | Unspecified† | Store A, Hold B | Store A, Hold B |
| H | H | | | X‡ | X | Input | Output | Store A in both registers | Store A in both registers |
| L | X | H or L | | X | X | Unspecified† | Input | Hold A, Store B | Hold, A Store B |
| L | L | | | X | X‡ | Output | Input | Store B in both registers | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-Time B̄ Data to A Bus | Real-Time B Data to A Bus |
| L | L | X | H or L | X | H | | | Stored B̄ Data to A Bus | Stored B Data to A Bus |
| H | H | X | X | L | X | Input | Output | Real-Time Ā Data to B Bus | Real-Time A Data to B Bus |
| H | H | H or L | X | H | X | | | Stored Ā Data to B Bus | Stored A Data to B Bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored Ā Data to B Bus and Stored B̄ Data to A Bus | Stored A Data to B Bus Stored B Data to A Bus |

* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors

† The data output functions may be enabled or disabled by various signals at the OE_{AB} or OE_{BA} inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|--------------------------------------|
| DC SUPPLY-VOLTAGE (V _{CC}) | -0.5 to 6 V |
| DC INPUT DIODE CURRENT, I _{IK} (for V _I < -0.5 V or V _I > V _{CC} + 0.5 V) | ±20 mA |
| DC OUTPUT DIODE CURRENT, I _{OK} (for V _O < -0.5 V or V _O > V _{CC} + 0.5 V) | ±50 mA |
| DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I _O (for V _O > -0.5 V or V _O < V _{CC} + 0.5 V) | ±50 mA |
| DC V _{CC} or GROUND CURRENT (I _{CC} or I _{GND}) | ±100 mA* |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55 to +100°C (PACKAGE TYPE E) | 500 mW |
| For T _A = +100 to +125°C (PACKAGE TYPE E) | Derate Linearly at 8 mW/°C to 300 mW |
| For T _A = -55 to +70°C (PACKAGE TYPE M) | 400 mW |
| For T _A = +70 to +125°C (PACKAGE TYPE M) | Derate Linearly at 6 mW/°C to 70 mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55 to +125°C |
| STORAGE TEMPERATURE (T _{stg}) | -65 to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum | +265°C |
| Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only | +300°C |

*For up to 4 outputs per device; add ± 25 mA for each additional output.

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RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTICS | LIMITS | | UNITS |
|---|--------|-----------------|-------|
| | MIN. | MAX. | |
| Supply-Voltage Range, V _{CC} *: (For T _A = Full Package-Temperature Range) | | | |
| AC Types | 1.5 | 5.5 | V |
| ACT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage, V _I , V _O | 0 | V _{CC} | V |
| Operating Temperature, T _A | -55 | +125 | °C |
| Input Rise and Fall Slew Rate, dt/dv | | | |
| at 1.5 V to 3 V (AC Types) | 0 | 50 | ns/V |
| at 3.6 V to 5.5 V (AC Types) | 0 | 20 | ns/V |
| at 4.5 V to 5.5 V (ACT Types) | 0 | 10 | ns/V |

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

STATIC ELECTRICAL CHARACTERISTICS: AC Series

| CHARACTERISTICS | TEST CONDITIONS | | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | | | UNITS | |
|--|--|--------|------------------------|--|------|------------|------|-------------|------|-------|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | | |
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| High-Level Input Voltage V _{IH} | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V | |
| | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | | |
| | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | | |
| Low-Level Input Voltage V _{IL} | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V | |
| | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | | |
| | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | | |
| High-Level Output Voltage V _{OH} | V _{IH} or V _{IL} | #, * } | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | | -0.05 | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | | -4 | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage V _{OL} | V _{IH} or V _{IL} | #, * } | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 0.05 | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 12 | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current I _I | V _{CC} or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA | |
| 3-State Leakage Current I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA | |
| Quiescent Supply Current, MSI I _{CC} | V _{CC} or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA | |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C. 75 ohms at +125°C.

CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

| CHARACTERISTICS | TEST CONDITIONS | | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | | | UNITS | |
|---|------------------|--|---------------------|--|------|------------|------|-------------|------|-------|----|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | | |
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| High-Level Input Voltage | V _{IH} | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V | |
| Low-Level Input Voltage | V _{IL} | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V | |
| High-Level Output Voltage | V _{OH} | V _{IH} or V _{IL} #,* | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage | V _{OL} | V _{IH} or V _{IL} #,* | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current | I _I | V _{CC} or GND | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA | |
| 3-State Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O =V _{CC} or GND | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA | |
| Quiescent Supply Current, MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load | ΔI _{CC} | V _{CC} -2.1 | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA | |

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#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

| INPUT | UNIT LOAD* |
|------------------|------------|
| CAB, CBA | 1.25 |
| SAB, SBA | 1.2 |
| OE _{AB} | 0.67 |
| OE _{BA} | 1.17 |
| An, Bn | 0.4 |

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

PREREQUISITE FOR SWITCHING: AC Series

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|------------------------------|------------------|------------------------|--|-------------|------------------|-------------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Max. Frequency | f _{max} | 1.5 3.3* 5† | 11 101 143 | — — — | 10 89 125 | — — — | MHz |
| Setup Time Data to Clock | t _{SU} | 1.5 3.3 5 | 27 3.1 2.2 | — — — | 31 3.5 2.5 | — — — | ns |
| Hold Time Data to Clock | t _H | 1.5 3.3 5 | 2 2 2 | — — — | 2 2 2 | — — — | ns |
| Clock Pulse Data to Clock | t _W | 1.5 3.3 5 | 44 4.9 3.5 | — — — | 50 5.6 4 | — — — | ns |

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|---|--|------------------------|--|---------------------|-----------------|---------------------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Store A Data to B Bus Store B Data to A Bus 652 | t _{PLH} t _{PHL} | 1.5 3.3* 5† | — 4.8 3.5 | 154 17.1 12.3 | — 4.7 3.4 | 169 18.9 13.5 | ns |
| Store A Data to B Bus Store B Data to A Bus 651 | t _{PLH} t _{PHL} | 1.5 3.3 5 | — 4.8 3.5 | 154 17.1 12.3 | — 4.7 3.4 | 169 18.9 13.5 | ns |
| A Data to B Bus B Data to A Bus 652 | t _{PLH} t _{PHL} | 1.5 3.3 5 | — 4 2.8 | 125 14 10 | — 3.9 2.8 | 138 15.4 11 | ns |
| A Data to B Bus B Data to A Bus 651 | t _{PLH} t _{PHL} | 1.5 3.3 5 | — 4 2.8 | 125 14 10 | — 3.9 2.8 | 138 15.4 11 | ns |
| Select to Data 652 | t _{PLH} t _{PHL} | 1.5 3.3 5 | — 4.3 3.1 | 136 15.3 10.9 | — 4.2 3 | 150 16.8 12 | ns |
| Select to Data 651 | t _{PLH} t _{PHL} | 1.5 3.3 5 | — 4.3 3.1 | 136 15.3 10.9 | — 4.2 3 | 150 16.8 12 | ns |
| 3-State Enabling/ Disabling Time Bus to Output or Register to Output | t _{PZL} t _{PZH} t _{PLZ} t _{PHZ} | 1.5 3.3 5 | — 5.2 3.5 | 154 18.4 12.3 | — 5.1 3.4 | 169 20.2 13.5 | ns |
| Power Dissipation Capacitance | C _{PD} § | — | 150 Typ. | | 150 Typ. | | pF |
| Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching) | V _{OH} V _{OHV} See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching) | V _{OL} V _{OLP} See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | C _I | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C _O | — | — | 15 | — | 15 | pF |

*3.3 V: min. is @ 3.6 V
max. is @ 3 V
†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
P_D = V_{CC}² C_{PD} f_i + Σ (V_{CC}² C_L f_o) where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

PREREQUISITE FOR SWITCHING: ACT Series

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|-----------------------------|------------------|------------------------|--|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Max. Frequency | f _{max} | 5* | 125 | — | 110 | — | MHz |
| Setup Time Data to Clock | t _{SU} | 5 | 2.2 | — | 2.5 | — | ns |
| Hold Time Data to Clock | t _H | 5 | 2 | — | 2 | — | ns |
| Clock Pulse Width | t _W | 5 | 3.9 | — | 4.5 | — | ns |

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|---|--|------------------------|--|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Store A Data to B Bus Store B Data to A Bus 652 | t _{PLH} t _{PHL} | 5* | 4 | 14.1 | 3.9 | 15.5 | ns |
| Store \bar{A} Data to B Bus Store \bar{B} Data to A Bus 651 | t _{PLH} t _{PHL} | 5 | 4 | 14.1 | 3.9 | 15.5 | ns |
| A Data to B Bus B Data to A Bus 652 | t _{PLH} t _{PHL} | 5 | 3.2 | 11.4 | 3.1 | 12.5 | ns |
| \bar{A} Data to B Bus \bar{B} Data to A Bus 651 | t _{PLH} t _{PHL} | 5 | 3.2 | 11.4 | 3.1 | 12.5 | ns |
| Select to Data 652 | t _{PLH} t _{PHL} | 5 | 3.7 | 13.2 | 3.6 | 14.5 | ns |
| Select to Data 651 | t _{PLH} t _{PHL} | 5 | 4 | 14.1 | 3.9 | 15.5 | ns |
| 3-State Enabling/ Disabling Time Bus to Output or Register to Output | t _{PZL} t _{PZH} t _{PLZ} t _{PHZ} | 5 | 4 | 14.1 | 3.9 | 15.5 | ns |
| Power Dissipation Capacitance | C _{PD} § | — | 150 Typ. | | 150 Typ. | | pF |
| Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching) | V _{OH} V _{OHV} See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching) | V _{OL} V _{OLP} See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | C _I | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C _O | — | — | 15 | — | 15 | pF |

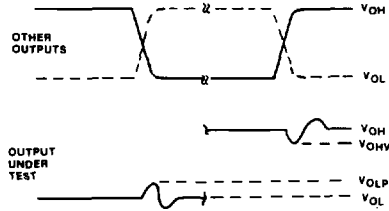
*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = V_{CC}^2 C_{PD} f_i + \sum V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$$

f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

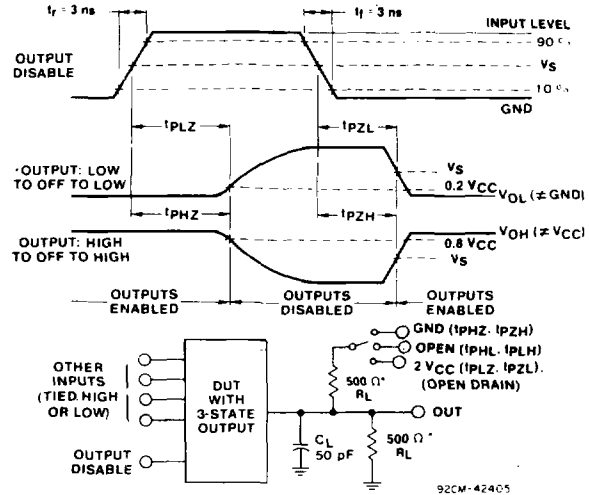
CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652



NOTES:
 1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
 2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
 PRR = 1 MHz, $t_r = 3$ ns, $t_f = 3$ ns, SKEW = 1 ns.
 3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH $0.1 \mu\text{F}$ CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

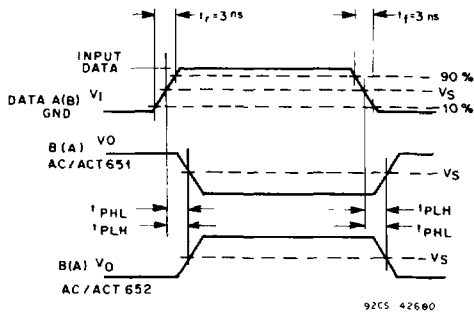
Fig. 1 - Simultaneous switching transient waveforms.



*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5$ V, $R_L = 1$ k Ω

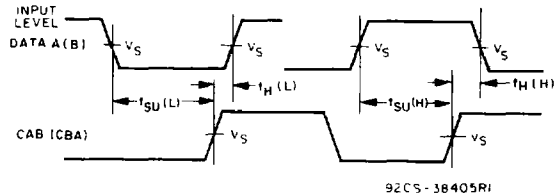
92CM-42405

Fig. 2 - Three-state propagation delay waveforms and test circuit.



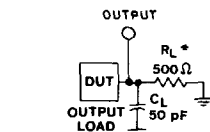
92CS-42680

Fig. 3 - Propagation delay times.



92CS-38405R1

Fig. 4 - Data setup and hold times.



*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5$ V, $R_L = 1$ k Ω

92CS-42589

Fig. 5 - Test circuit.

| | CD54/74AC | CD54/74ACT |
|---------------------------------|--------------|--------------|
| Input Level | V_{CC} | 3 V |
| Input Switching Voltage, V_S | 0.5 V_{CC} | 1.5 V |
| Output Switching Voltage, V_S | 0.5 V_{CC} | 0.5 V_{CC} |