MINDSPEED™
BUILD IT FIRST

M02049/M02050

3.3/5V Limiting Amplifier for Applications to 4.3 Gbps

Data Sheet

TABLE OF CONTENTS

3.3/5V Limiting Amplifier for Applications to 4.3 Gbps

FEATURES

- Operates with a 3.3 or 5V supply
- 4 mV input sensitivity at 2.5 Gbps
- CML output version (M02049) or PECL output version (M02050)
- Rate Selection for ≤ 1.25 Gbps operation
- Average Receive power monitor output ($RSSI_{AVG}$)
- Peak-to-peak Receive power monitor output ($RSSI_{PP}$)
- On-chip DC offset cancellation circuit
- Low power (< 80 mW at 3.3V, CML version)
- Programmable CML Output Amplitude Level
- Output Jam function
- 16-pin 3x3 mm QFN package

APPLICATIONS

- 2.5 Gbps STM-16/OC-48 SDH/SONET
- 1.06, 2.12 and 4.24 Gbps Fibre Channel
- 1.25 Gbps Ethernet
- 2.67 Gbps SDH/SONET with FEC

DESCRIPTION

The M02049/50 are integrated high-gain limiting amplifiers. Featuring CML outputs, the M02049 is useable in applications to 4.3 Gbps while the M2050 features PECL outputs and is intended for use in applications to 2.5 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02049/50 can operate with a 3.3V or 5V supply.

Rate select is supported for SFP applications and/or to achieve optimum sensitivity at data rates ≤ 1.25 Gbps. When rate select is high, optimum sensitivity is achieved at 2.5 Gbps and operation up to 4.3 Gbps (M02049) is possible with reduced sensitivity.

The M02049/50 also includes two analog RSSI outputs proportional to either the average or peak to peak input signal and a programmable signal-level detector allowing the user to set thresholds at which the logic outputs are enabled.

TABLE 1 ORDERING INFORMATION

Part Number	Pin Package
M02049	CML Outputs in QFN16 package
M02050	PECL Outputs in QFN16 package
M02049-EVM	Evaluation board with M02049
M02050-EVM	Evaluation board with M02050

TOP LEVEL DIAGRAM

Fig. 1

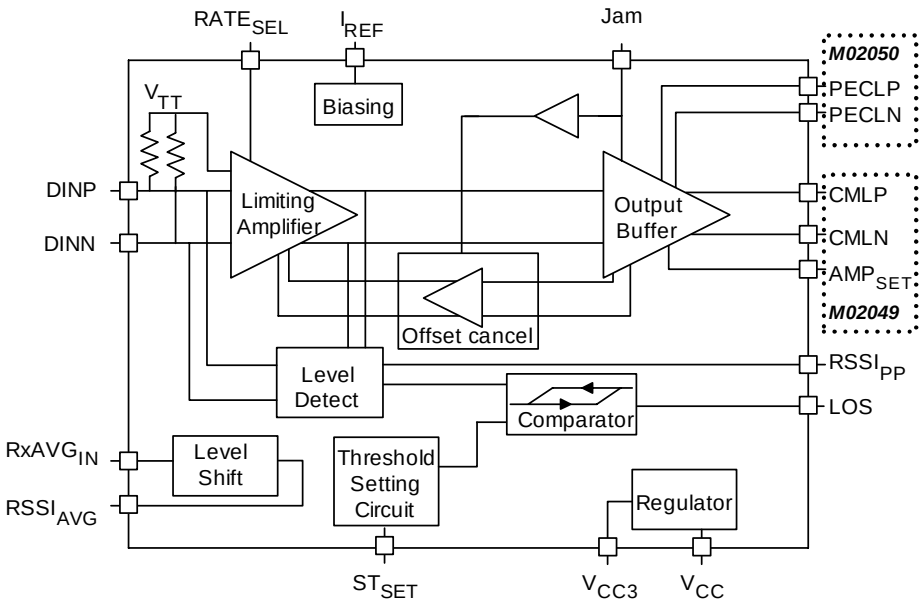


TABLE 2 PIN DESCRIPTIONS

QFN Pin# (M02049)	QFN Pin# (M02050)	Name	Function
1	---	AMP_{SET}	CML Output amplitude adjustment. Enables setting output swing of CML outputs from 400mV$_{PP}$ to 800mV$_{PP}$ differential with an external resistor to ground. When grounded, output swing is at the minimum level (400mV$_{PP}$ differential). Note that this pad must be connected to ground for proper output swing with PECL outputs (M02050).
---	1	GND	Ground.
2	2	V_{CC}	Power supply. Connect to either +5V or +3.3V.
3	---	CMLN	Inverting data output (CML).
4	---	CMLP	Non-inverting data output (CML).
---	3	PECLN	Inverting data output (PECL).
---	4	PECLP	Non-inverting data output (PECL).
5	5	I_{REF}	Internal reference current. Must be connected to ground through a 12.1kΩ 1% resistor.
6	6	ST_{SET}	Loss of signal threshold setting input. Connect a 1% resistor between this pin and V_{CC3} to set loss of signal threshold.
7	7	V_{CC3}	Power supply input for 3.3V applications or the output of the internally regulated 3.3V voltage when V_{CC} = 5V. Connect directly to supply for 3.3V applications (internal regulator not in use). Do not connect to power supply if V_{CC} = 5V.
8	8	$RATE_{SEL}$	Rate select. When low or floating, the device is in low-rate mode (data rates ≤ 1.25 Gbps) and has reduced bandwidth. When high, the device is in full-rate mode with full bandwidth. Internal 80kΩ resistor to ground.
9	9	DINP	Non-inverting data input. Internally terminated with 50Ω to V_{TT}.
10	10	DINN	Inverting data input. Internally terminated with 50Ω to V_{TT}.
11	11	GND	Ground.
12	12	$RxAVG_{IN}$	Average power monitor input. Connect to monitor output of TIAs that produce a current (sink) mirror replica of the photodiode current. Leave floating if not used.
13	13	JAM	Output disable. When high, data outputs are disabled (with non-inverting output held high and inverting output held low). Connect to LOS output to disable outputs with loss of signal. Outputs are enabled when JAM is low or floating. Internal 150kΩ resistor to ground.

TABLE 2 PIN DESCRIPTIONS

QFN Pin# (M02049)	QFN Pin# (M02050)	Name	Function
14	14	LOS	Loss of signal output. Goes high when input signal falls below threshold set by ST_{SET}. Open collector TTL with internal 80kΩ pull-up resistor to V_{CC}.
15	15	$RSSI_{AVG}$	Receiver average input power monitor. Provides a current source mirror of the current at $RxAVG_{IN}$. Connect a resistor to ground to set the full scale voltage to the desired level at maximum average input power.
16	16	$RSSI_{PP}$	Receiver peak-to-peak input voltage monitor. Provides a DC voltage (ground referenced) proportional to the peak-to-peak input voltage swing.
17	17	Center Pad	Ground. Must be connected to ground for proper operation.

TABLE 3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage (V_{CC}-GND)	-0.5 to +6V	V
T_{STG}	Storage temperature	-65 to +150	°C
CMLP, CMLN	CML Output pins voltage	V_{CC} - 0.4 to V_{CC} + 0.4	V
PECLP, PECLN	PECL Output pins voltage	V_{CC} - 0.4 to V_{CC} + 0.4	V
|DINP - DINN|	Data input pins differential voltage	0.80	V
DINP, DINN	Data input pins voltage meeting |DINP - DINN| requirement	GND to V_{CC3} + 0.4	V
I(AMP_{SET})	Current into AMP_{SET} output	+ 0 to -160	µA
ST_{SET}	Signal detect threshold setting pin voltage	GND to V_{CC} + 0.4	V
JAM	Output enable pin voltage	GND to V_{CC} + 0.4	V
LOS	Status Output pins voltage	GND to V_{CC} + 0.4	V
Rate_Sel	Rate Select input pin voltage	GND to V_{CC} + 0.4	V
I_{REF}	Current into Reference input	+ 0 to -120	µA
I($RSSI_{AVG}$)	Current into RSSIavg input	+ 0 to -3	mA
$RSSI_{PP}$	$RSSI_{PP}$ pin voltage	GND to +3.6	V
I(LOS)	Current into Loss of Signal pin	+1500 to -100	µA

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Note: The package bottom must be adequately grounded to ensure correct thermal and electrical performance, and it is recommended that vias are inserted through to a lower ground plane.

TABLE 4 RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Units
Power supply: (V_{CC}-GND) (apply no potential to V_{CC3}) or (V_{CC3}-GND) (connect V_{CC} to same potential as V_{CC3})	+5V ± 7.5% or +3.3V ± 7.5%	V
Junction temperature	-40 to +110	°C
Operating ambient	-40 to +85	°C

TABLE 5 DC CHARACTERISTICS

V_{CC} = +3.3V ± 7.5% or +5V ± 7.5%, T_A = -40°C to +85°C, unless otherwise noted.
Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	Outputs terminated into 50Ω to V_{CC} 400mV$_{PP}$ differential (CML version) 800mV$_{PP}$ differential (CML version) PECL (includes PECL load)		23 29 52		mA
V_{OUTL0}	CML Output Low Voltage	Single ended, 50Ω load to V_{CC}; R_{AMPSET} = 0Ω; 10mV$_{PP}$ input	V_{CC}-0.22	V_{CC}-0.2	V_{CC}-0.18	V
V_{OUTH0}	CML Output High Voltage	Single ended, 50Ω load to V_{CC}; R_{AMPSET} = 0Ω; 10mV$_{PP}$ input	V_{CC}-0.02	V_{CC}	V_{CC}	V
$V_{OUTL604}$	CML Output Low Voltage	Single ended, 50Ω load to V_{CC}; R_{AMPSET} = 604Ω; 10mV$_{PP}$ input	V_{CC}-0.45	V_{CC}-0.4	V_{CC}-0.35	V
$V_{OUTH604}$	CML Output High Voltage	Single ended, 50Ω load to V_{CC}; R_{AMPSET} = 604Ω; 10mV$_{PP}$ input	V_{CC}-0.04	V_{CC}	V_{CC}	V
$V_{OUTLpecl}$	PECL Output Low Voltage (PECLP, PECLN)	Single ended; 50Ω load to V_{CC}-2V	V_{CC}-1.81	V_{CC}-1.71	V_{CC}-1.62	V
$V_{OUTHpecl}$	PECL Output High Voltage (PECLP, PECLN)	Single ended; 50Ω load to V_{CC}-2V	V_{CC}-1.025	V_{CC}-0.952	V_{CC}-0.88	V
	Differential Input Resistance	Measured between DINP and DINN	85	100	115	Ω
	Differential Output Resistance	Measured between CMLP and CMLN	170	200	230	Ω
	LOS Output High Voltage	External 4.7-10kΩ pull up to V_{CC}	2.4	V_{CC}		V
	LOS Output Low Voltage	External 4.7-10kΩ pull up to V_{CC}	0		0.4	V
	Logic Input High Voltage JAM, RATE$_{SEL}$		2.7		5.5	V
	Logic Input Low Voltage JAM, RATE$_{SEL}$				0.8	V

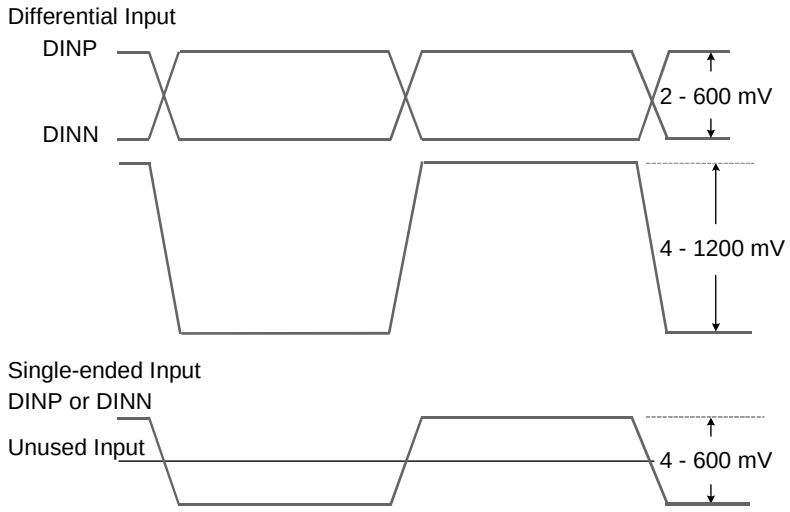
TABLE 6 AC CHARACTERISTICS

V_{CC} = +3.3V ± 7.5% or +5V ± 7.5%, T_A = -40°C to +85°C, input bit rate = 2.5 Gbps 2^{23}-1 PRBS unless otherwise noted.
Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(MIN))}$	Differential Input Sensitivity	2.5 Gbps, BER < 10^{-12}			4	mV
		3.3 Gbps, BER < 10^{-12}		5		mV
		4.3 Gbps, BER < 10^{-12}		6		mV
$V_{I(MAX)}$	Input Overload	BER < 10^{-12}, differential input 2.5 Gbps	1200			mV
		BER < 10^{-12}, single-ended input, 2.5 Gbps	600			mV
v_n	RMS Input Referred Noise	$RATE_{SEL}$ = high		185		μV_{RMS}
V_{SD}	Signal Detect Programmable Range	Differential inputs	4		100	mV
HYS	Signal Detect Hysteresis	(electrical); signal detect level set to 20 mV p-p	2	4	6	dB
RSSIpp	Peak-to-peak received signal strength indicator range		4		100	mV
RSSIave	Average received signal strength indicator range	± 15% accuracy ± 20% accuracy	5 0.5		500 2	µA mA
BW_{LF}	Small-Signal –3dB Low Frequency Cutoff	Excluding AC coupling capacitors		25		kHz
DJ	Deterministic Jitter	K28.5 pattern at 3.3 Gbps (CML version) K28.5 pattern at 2.125 Gbps (PECL version)			25 25	ps
RJ	Random Jitter	10mV_{PP} input		3		ps_{RMS}
t_r / t_f	Data Output Rise and Fall Times	20% to 80%; outputs terminated into 50Ω; 10mV_{PP} input $RATE_{SEL}$ = High, CML Low Swing $RATE_{SEL}$ = High, CML High Swing & PECL $RATE_{SEL}$ = Low, CML and PECL		 80 90 185	 110 300	ps
$T_{RATESEL}$	Rate select assert / deassert time	Time from when rate select is asserted high or low until amplifier is performing at selected bandwidth			10	µs
T_{LOS_ON}	Time from LOS state until LOS output is asserted	LOS assert time after 1Vp-p input signal is turned off; signal detect level set to 10mV			100	µs
T_{LOS_OFF}	Time from non-LOS state until LOS is deasserted	LOS deassert time after input crosses signal detect level; signal detect set to 10mV with applied input signal of 20mV_{PP}			100	µs

DATA INPUT REQUIREMENTS

Fig. 2

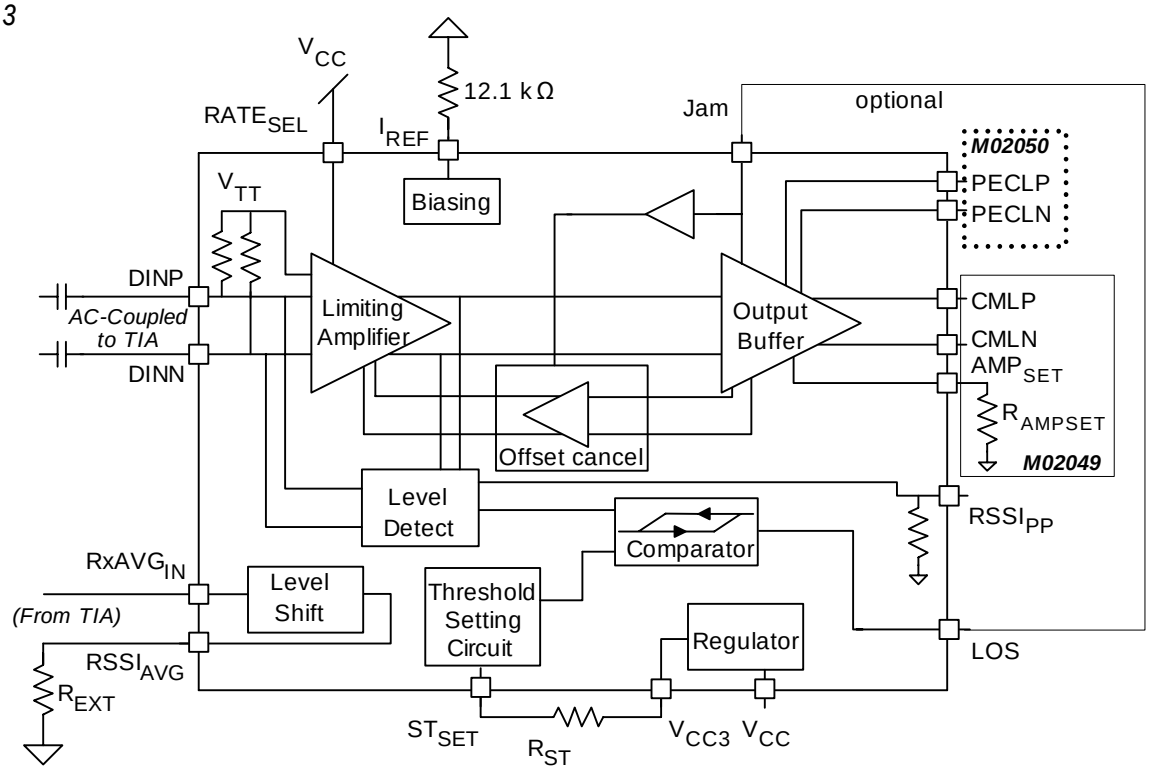


Note:

For single-ended input connections.
When connecting to the used input with AC-coupling, the unused input should be AC-coupled through 50 Ω to the supply voltage of the TIA;
When connecting to the used input with DC-coupling, the unused input should be DC-coupled through 50 Ω to a voltage equal to the common mode level of the used input.

TYPICAL APPLICATIONS CIRCUIT

Fig. 3



Note:
Applies for V_{CC} = 5V or 3.3V. AC-coupled inputs shown.
If not using $RxAVG_{IN}$, then let it float (no connect) and also $RSSI_{AVG}$ out should float (no connect).
R_{AMPSET} only applies for CML operation. For PECL operation R_{AMPSET} = 0 Ω.
$RATE_{SEL}$ shown for high bandwidth operation, for input data rates ≤ 1.25 Gbps, $RATE_{SEL}$ should float (no connect).

Overview

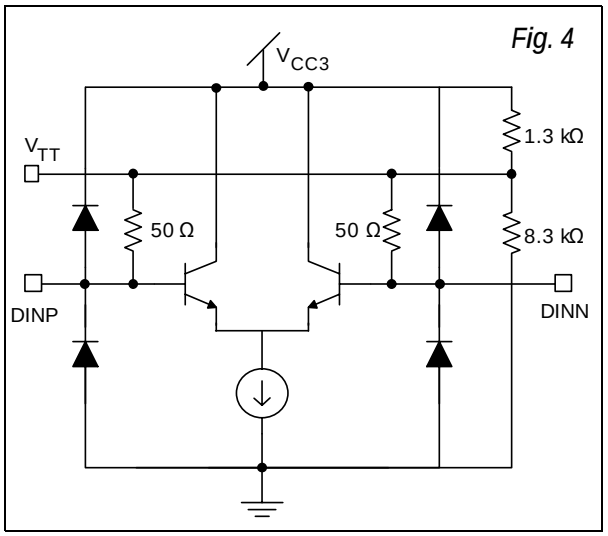
The M02049 is a high-gain limiting amplifier for applications up to 4.3 Gbps (2.5 Gbps M02050), and incorporates a limiting amplifier, an input signal level detection circuit and also a fully integrated DC-offset cancellation loop that does not require any external components. The M02049 features a CML output buffer and the user is provided with the flexibility to set the CML output amplitude levels. The M02050 features PECL data outputs.

Both versions provide the user with the flexibility to set the signal detect threshold. Optional output buffer disable (squelch/jam) can be implemented using the JAM input.

Inputs (Fig. 4)

The data inputs are internally connected to V_{TT} via 50 Ω resistors, and generally need to be AC coupled. Referring to Fig. 4, the nominal V_{TT} voltage is 2.85V because of the internal resistor divider to V_{CC3}, which means this is the DC potential on the data inputs. See the applications information section for further details on choosing the AC-coupling capacitor.

CML DATA INPUTS



DC Offset Compensation

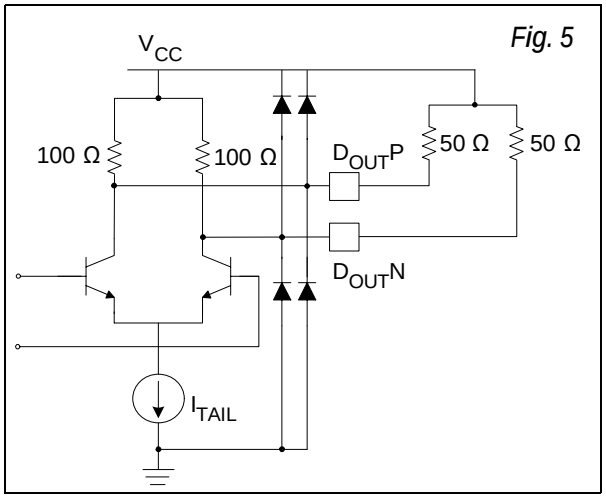
The M02049/50 contain an internal DC autozero circuit that can remove the effect of DC offsets without using external components. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off is typically 25 kHz.

Data Outputs (Fig. 5 and Fig. 6)

CML Outputs (M02049)

The basic CML output configuration is shown in Fig. 5. The external resistor R_{AMPSET} controls the value of I_{TAIL}. The output swing is linearly proportional to the value of R_{AMPSET}. It is possible to set the output voltage swing linearly between 400 mVpp differential and 800 mVpp differential, when the outputs are properly terminated. See the applications information section for further details on setting the output swing amplitude.

CML DATA OUTPUTS (M02049)



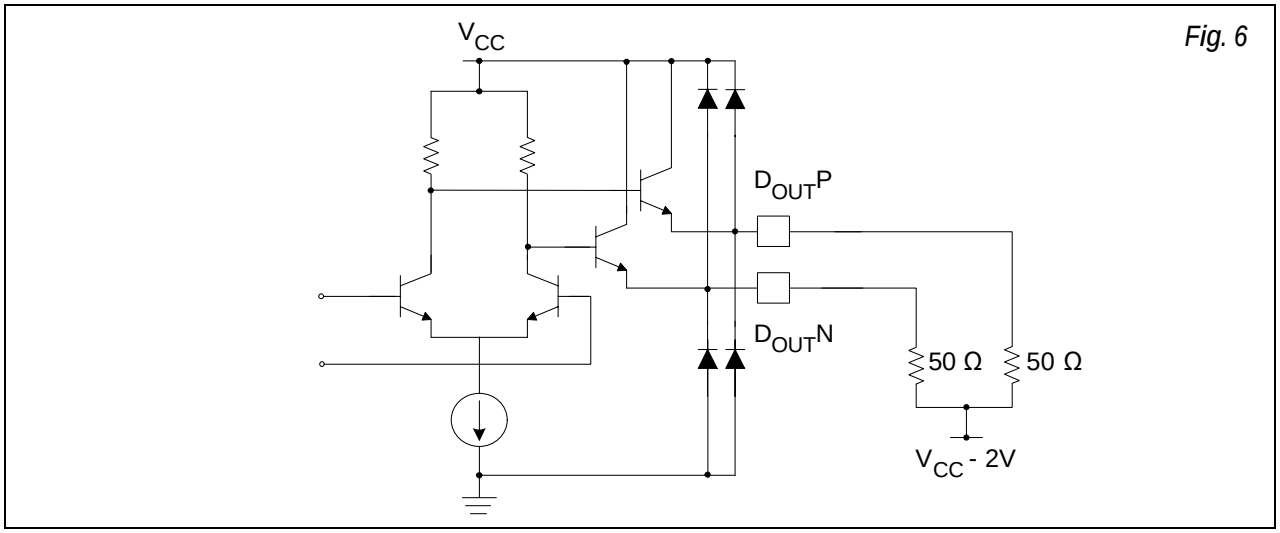
PECL Outputs (M02050)

The M02050 features 100k/300k PECL compliant outputs as shown in Fig. 6. The outputs may be terminated using any standard AC or DC-coupling PECL termination technique. AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drive and compatibility with non-PECL interfaces.

FUNCTIONAL DESCRIPTION

PECL DATA OUTPUTS (M02050)

Fig. 6

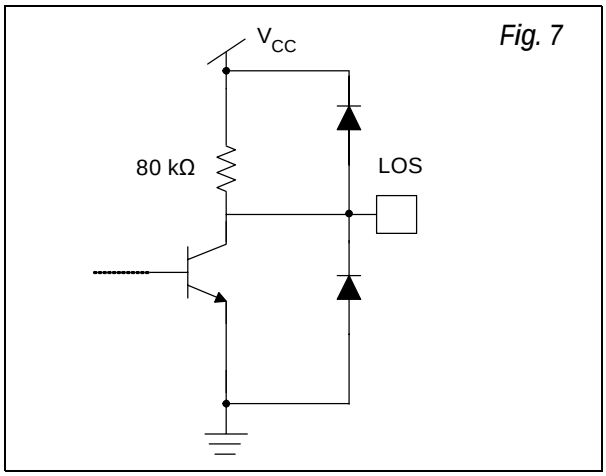


Loss of Signal (LOS) (Fig. 7 and Fig. 8)

The M02049/50 features input signal level detection over an extended range. Using an external resistor, R_{ST}, between pin ST_{SET} and V_{CC3} (Fig. 8) the user can program the input signal threshold. The signal detect status is indicated on the LOS output pin shown in Fig. 7. The LOS signal is active when the signal is below the threshold value. The signal detection circuitry has the equivalent of 4dB (typical) electrical hysteresis.

LOS OUTPUT

Fig. 7



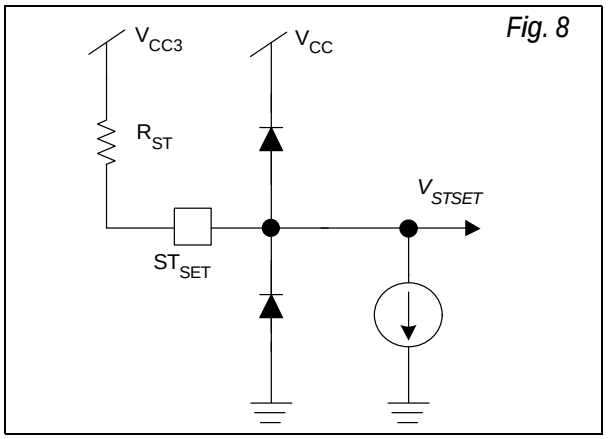
R_{ST} establishes a threshold voltage at the ST_{SET} pin as shown in Fig. 8. Internally, the input signal level is monitored by the Level Detector (which also outputs the $RSSI_{PP}$ voltage). As described in the $RSSI_{PP}$ section, this voltage is proportional to the input signal peak to peak value. The voltage at ST_{SET} is internally compared to the signal level from the Level Detector. When the Level Detect voltage is less than $V_{(STSET)}$, LOS is asserted and will stay asserted until the input signal level increases by a predefined amount of hysteresis. When the input level increases by more than this hysteresis above $V_{(STSET)}$, LOS is deasserted. See the applications information section for the selection of R_{ST}.

Note that ST_{SET} can be left open if the loss of signal detector function is not required. In this case LOS would be low.

FUNCTIONAL DESCRIPTION

STSET INPUT

Fig. 8

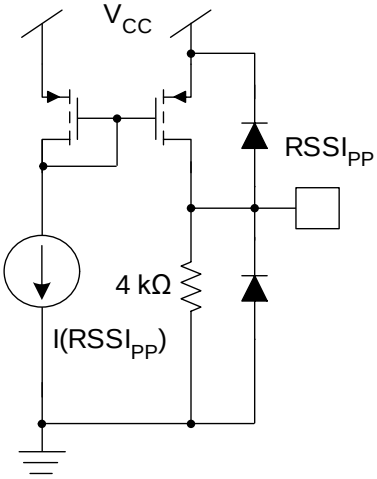


Peak to Peak Received Signal Strength Indicator ($RSSI_{PP}$) (Fig 9).

The $RSSI_{PP}$ output voltage is proportional to the peak to peak level of the input signal. It is not necessary to connect an external capacitor to this output. Internally, the RSSI voltage is compared with a user selectable reference to determine loss of signal as described in the previous section.

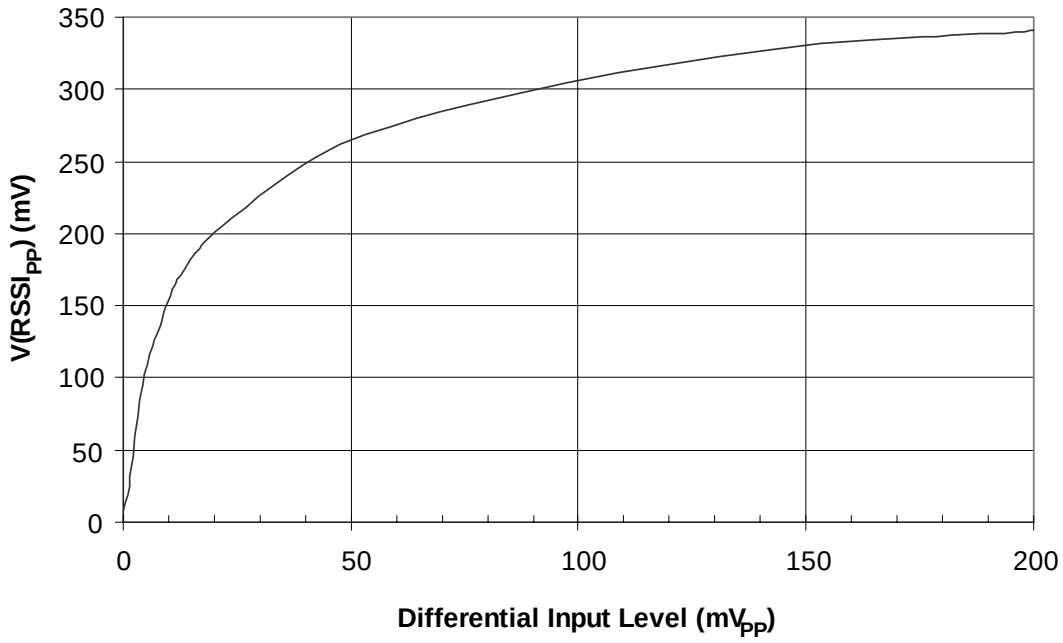
$RSSI_{PP}$ OUTPUT

Fig. 9



$RSSI_{PP}$ TRANSFER FUNCTION

Fig. 10



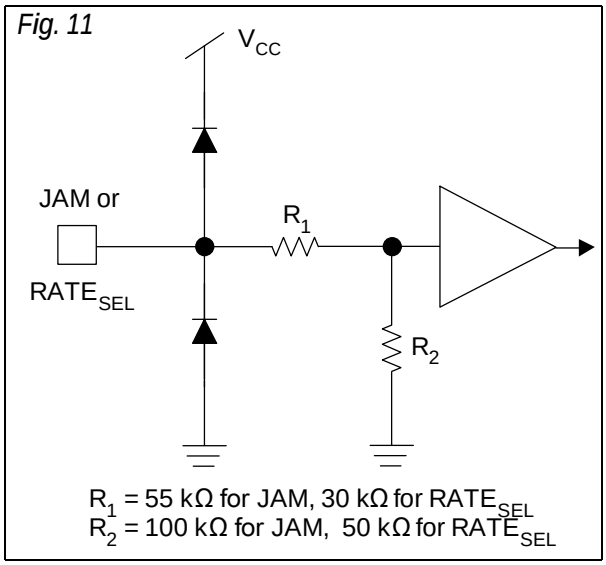
JAM Function (Fig. 11)

When asserted, the active high power down (JAM) pin forces the outputs to a logic “one” state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the threshold. The function is normally used to allow data to propagate only when the signal is above the user's bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present (“squelch”).

In order to implement this function, LOS should be connected to the JAM pin shown in Fig. 11, thus forcing the data outputs to a logic “one” state when the signal falls below the threshold.

JAM & $RATE_{SEL}$ INPUT

Fig. 11



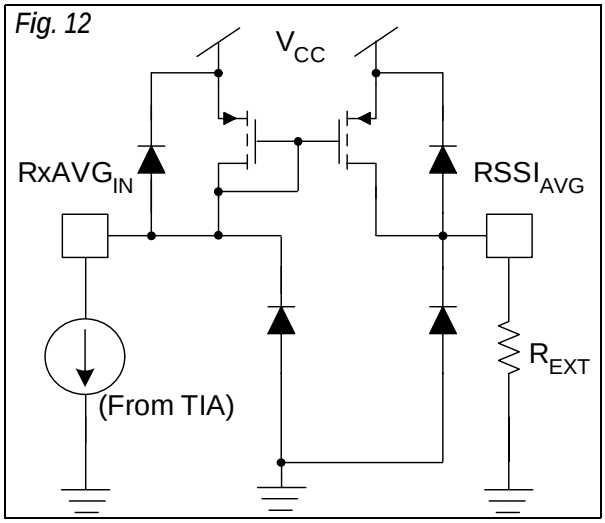
R_1 = 55 kΩ for JAM, 30 kΩ for $RATE_{SEL}$
R_2 = 100 kΩ for JAM, 50 kΩ for $RATE_{SEL}$

Average Received Signal Strength Indicator ($RSSI_{AVG}$) (Fig. 12)

The $RSSI_{AVG}$ output current is a mirrored version of the $RxAVG_{IN}$ current from compatible TIAs. It sources rather than sinks the current making it compatible with DDMI type interfaces.

$RSSI_{AVG}$ OUTPUT

Fig. 12



Voltage Regulation

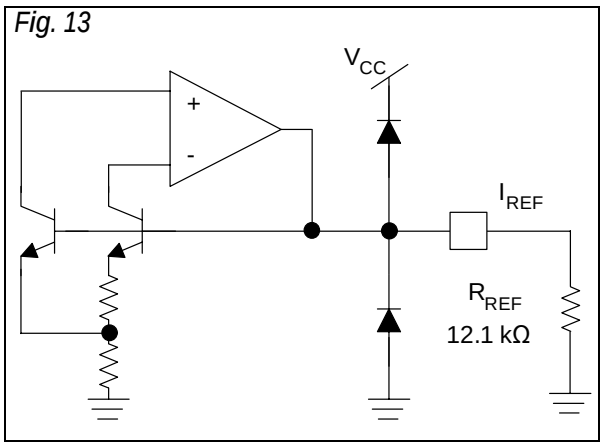
The M02049/50 contain an on-chip voltage regulator to allow both 5V and 3.3V operation. When used at 5V, the on-chip regulator is enabled and the digital inputs and outputs are compatible with TTL 5V logic levels.

Reference Current Generation (Fig. 13)

The M02049/50 contain an accurate on-chip bias circuit that requires an external 12.1 kΩ 1% resistor, R_{REF}, from pin I_{REF} to ground to define an on-chip reference current.

REFERENCE CURRENT CONNECTION

Fig. 13



Connecting V_{CC} and V_{CC3}

For 5V operation, the V_{CC} pin is connected to an appropriate 5V ± 7.5% supply. No potential should be applied to the V_{CC3} pin. The only connection to V_{CC3} should be R_{ST} as shown in Fig. 8.

When V_{CC} = 5V all logic outputs and the data outputs are 5V compatible while the CML data inputs are still referenced to 3.3V from the internal regulator (see Fig. 4). For low power operation, V_{CC} and V_{CC3} should be connected to an appropriate 3.3V ± 7.5% supply. In this case all I/Os are 3.3V compatible.

Choosing an Input AC-Coupling Capacitor

When AC-coupling the input the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number of consecutive identical bits, and the input resistance of the part. For SONET data, a good rule of thumb is to chose a coupling capacitor that has a cut-off frequency less than 1/(10,000) of the input data rate. For example, for 2.5 Gbps data, the coupling capacitor should be chosen as:

$f_{CUTOFF} \leq (2.5x10^9 / 10x10^3) = 250x10^3$

The -3 dB cutoff frequency of the low pass filter at the 50 Ω input is found as:

$f_{3dB} = 1/ (2 * \pi * 50\ \Omega * C_{AC})$
so solving for C where $f_{3dB} = f_{CUTOFF}$

$$C_{AC} = 1/ (2 * \pi * 50\ \Omega * f_{CUTOFF}) \quad \text{EQ.1}$$

and in this case the minimum capacitor is 12 nF.

For Ethernet or Fibre Channel, there are less consecutive bits in the data, and the recommended cut-off frequency is 1/(1,000) of the input data rate. This results in a minimum capacitor of 1.5 nF for 2.125 Gbps Fibre Channel.

Multirate applications down to 155 Mbps

In this case, the input coupling capacitor needs to be large enough to pass 15 kHz ($155x10^6$/10,000) which results in a capacitor value of 0.2 µF. However, because this low pass frequency is close to the 25 kHz low pass frequency of the internal DC servo loop, it is preferable to use a larger input coupling capacitor such as 1 µF which provides an input cutoff frequency of 3.1 kHz. This separates the two poles sufficiently to allow them to be considered independent. This capacitor should also have a 10 nF capacitor in parallel to pass the higher frequency data (in the multirate application) without distortion.

In all cases, a high quality coupling capacitor should be used as to pass the high frequency content of the input data stream.

Using Rate Selection

When the $RATE_{SEL}$ pin (shown in Fig. 11) is tied high, the M02049 bandwidth is set to its maximum which allow the M02049 to operate at data rates up to 4.3 Gbps. Because of the performance of PECL outputs, the M02050 should not be used at data rates above 2.5 Gbps. When operating at data rates ≤ 1.25 Gbps, then $RATE_{SEL}$ should be tied low or left floating. This enables low-rate mode which reduces the bandwidth (and thus the noise level) of the part.

Using RSSI$_{AVG}$

As shown in the typical applications circuit (Fig. 3), when interfacing to a TIA that features a "MON" output such as the M02010 or M02013, the M02049/50 can reference the current sunk into the TIA "MON" output and produce a proportional current at the 2049/50 RSSI$_{AVG}$ output. The current is sourced into resistor R_{EXT} to ground creating a voltage suitable for DDMI applications. R_{EXT} should be chosen as:

R_{EXT} = 1/(maximum current into RSSI$_{AVG}$) EQ.2

This keeps the voltage at RSSI$_{AVG}$ between 0 and 1 V.

Setting the CML Output Swing Level (M02049)

The CML output circuit is shown in Fig 5. It is basically a differential pair with a tail current of I_{TAIL}. The load of the differential pair is formed by the parallel combination of R_{OUT} and R_{LOAD} for high frequencies where the output AC-coupling capacitor can be considered as a short circuit (100 || 50 = 33.3 Ω). The single-ended output voltage swing is given by EQ.3:

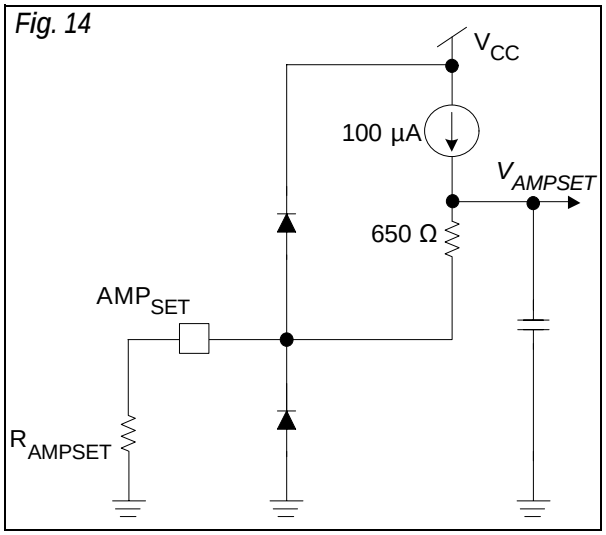
$V_{PP\text{-}SE} = I_{TAIL} \times (R_{OUT} \parallel R_{LOAD})$ EQ.3

The required minimum voltage swing sets I_{TAIL} and I_{TAIL} determines the output power consumption. The minimum voltage swing depends on the application. Therefore, M02049 provides the user the flexibility to optimize the voltage swing and the output power consumption for the application by setting I_{TAIL} using an external resistor (R_{AMPSET}) shown in Fig. 14. To select the required swing, use the following equation (EQ.4):

$I_{TAIL} = 6\text{ mA} + (R_{AMPSET} \times 10.0 \times 10^{-3})\text{ mA}$ EQ.4

AMPSET

Fig. 14



The minimum I_{TAIL} is 6mA and occurs when the AMPSET pin is directly connected to ground. The resulting voltage swing is approximately 200 mVpp, single-ended (= 6 mA x 33 Ω). This is sufficient for most applications. If it is necessary, the voltage swing can be increased at the expense of the power consumption by connecting an external resistor R_{AMPSET} between the AMP_{SET} pin and ground. The value of R_{AMPSET} can be calculated from EQ.4. A resistor of 604 Ω results in 12 mA tail current which delivers an approximate voltage swing of 400 mVpp, single-ended (12 mA x 33 Ω).

APPLICATIONS INFORMATION

Setting the Signal Detect Level

Using Fig. 15, the value for R_{ST} is chosen to set the LOS threshold at the desired value. The resulting hysteresis is also shown in Fig. 15.

From Fig. 15, it is apparent that small variations in R_{LOS} cause significant variation in the LOS threshold level, particularly for low input signal levels. This is because of the logarithmic relationship between the RSSI voltage and the input signal level. It is recommended that a 1% resistor be used for R_{ST} and that allowance is provided for LOS variation, particularly when the LOS threshold is near the sensitivity limit of the M02049.

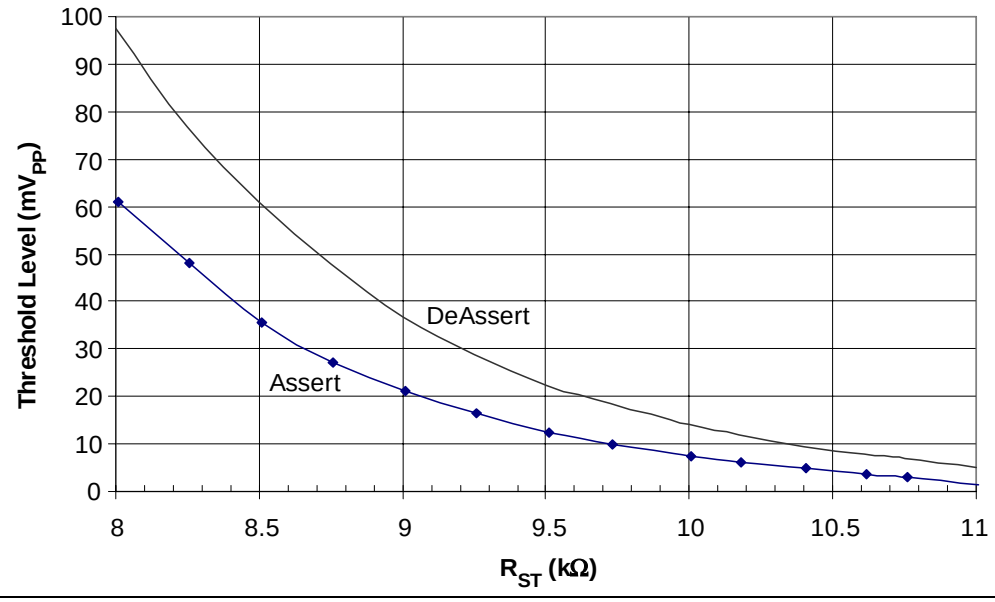
Example R_{ST} resistor values are given in Table 7.

TABLE 7 — R_{ST} RESISTOR VALUES

VIN (mV pp) differential	R_{ST} (kΩ)
6.6	10.2
13	9.53
20	9.10
39	8.45
60	8.06

LOSS OF SIGNAL CHARACTERISTIC

Fig. 15



APPLICATIONS INFORMATION

PECLP and PECLN Termination (M02050)

The outputs of the M02050 are PECL compatible and any standard AC or DC-coupling termination technique can be used. Fig. 16 and 17 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drift and compatibility with non-PECL interfaces. Fig. 16 shows the circuit configuration and Table 8 lists the resistor values. If using transmission lines other than 50 Ω, the shunt terminating resistance Z_T should equal twice the impedance of the transmission line (Z_O).

DC-coupling can be used when driving PECL interfaces and has the advantage of a reduced component count. A Thevenin termination is used at the receive end to give a 50 Ω load and the correct DC bias. Fig. 17 shows the circuit configuration and Table 8 the resistor values.

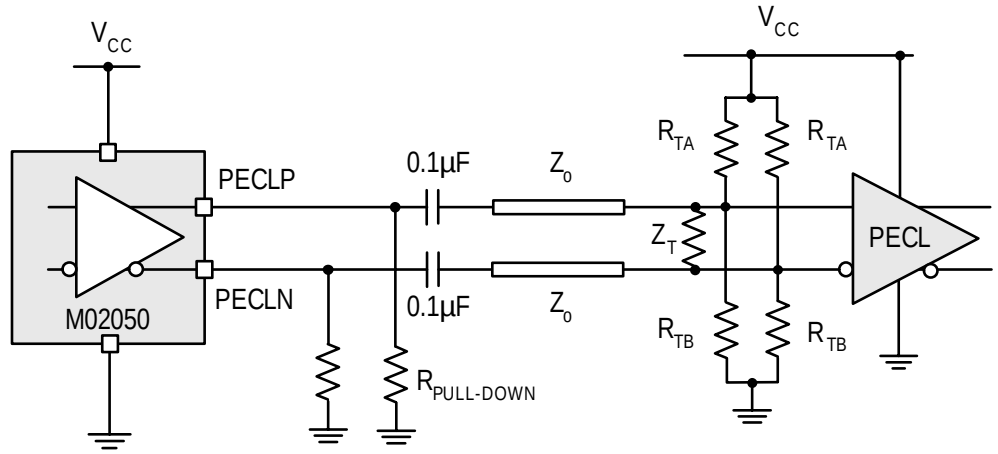
Alternatively, if available, terminating to V_{CC} - 2V as shown in Fig. 18 has the advantage that the resistance value is the same for 3.3 V and 5 V operation and it also has performance advantages at high data rates.

TABLE 8 PECL TERMINATION RESISTOR VALUES

Supply	Output Impedance	$R_{PULL-DOWN}$	Z_T	R_{TA} / R_{TB}	R_T / R_B
5 V	50 Ω	270 Ω	100 Ω	2.7 kΩ / 7.8 kΩ	82 Ω / 130 Ω
3.3 V	50 Ω	150 Ω	100 Ω	2.7 kΩ / 4.3 kΩ	130 Ω / 82 Ω

AC-COUPLED PECL TERMINATION

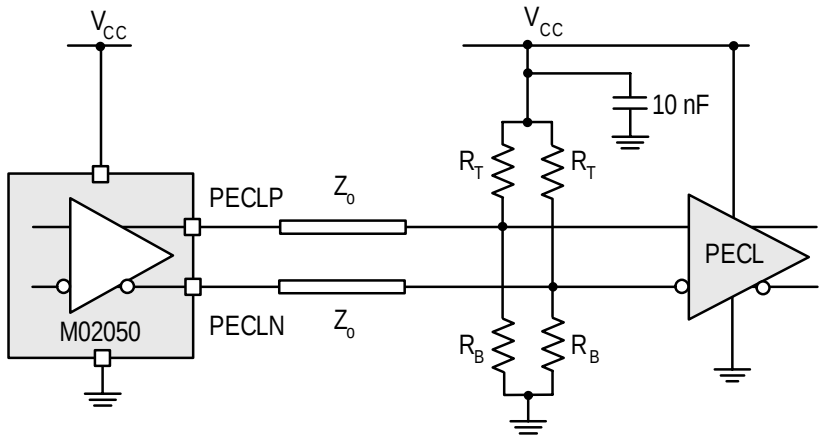
Fig. 16



APPLICATIONS INFORMATION

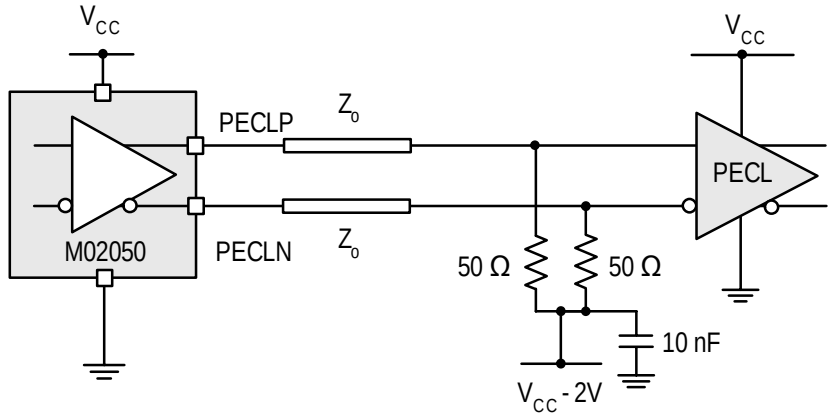
DC-COUPLED PECL TERMINATION

Fig. 17



ALTERNATIVE PECL TERMINATION

Fig. 18

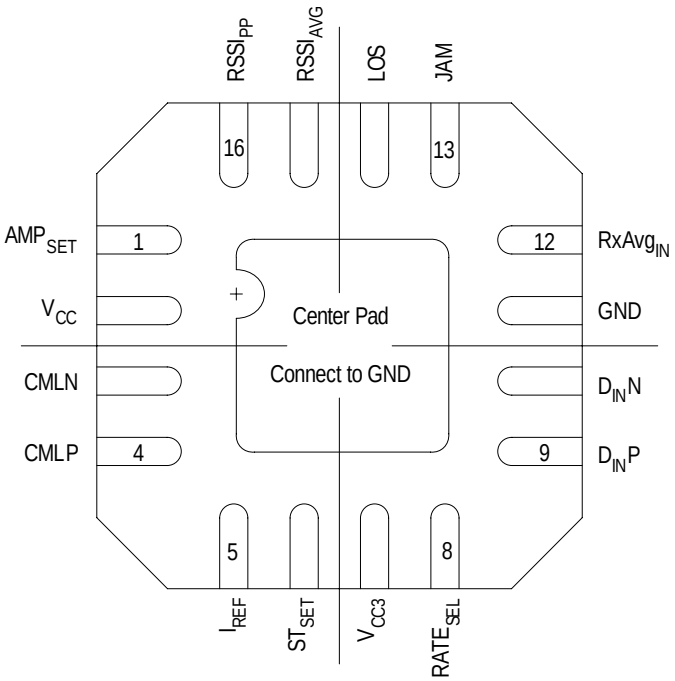


PACKAGE PINOUT

M02049 PINOUT

Fig. 19

16 Pin (3 x 3mm)
QFN top view



M02050 PINOUT

Fig. 20

16 Pin (3 x 3mm)
QFN top view

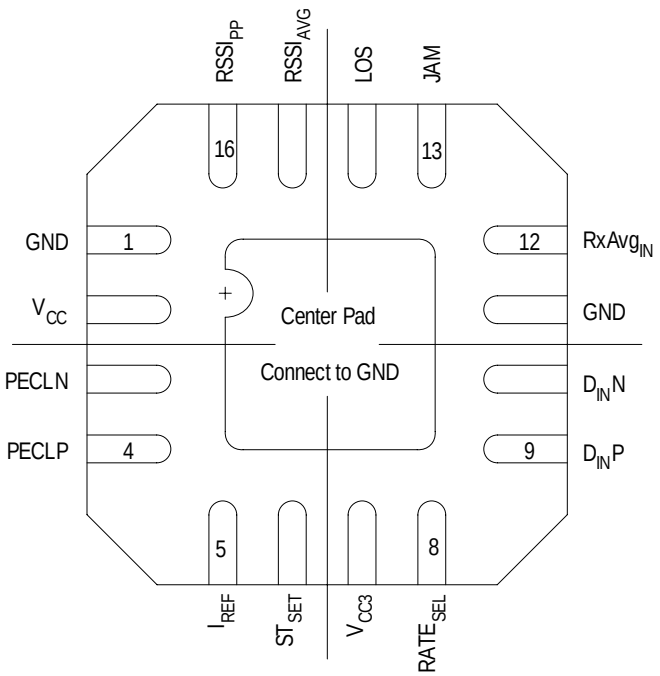
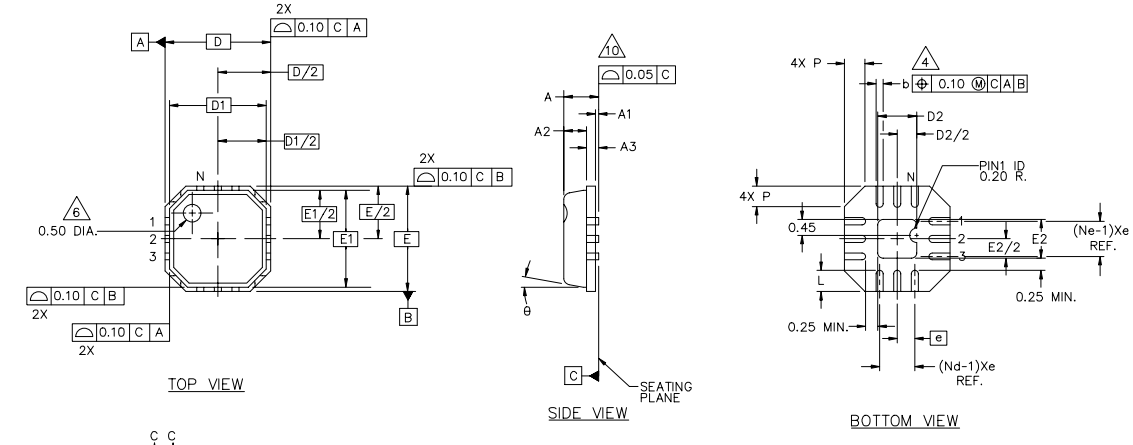
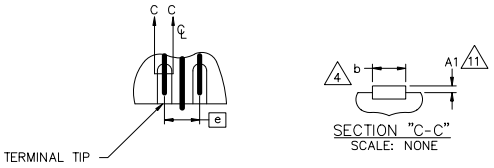


Fig. 21





FOR EVEN TERMINAL/SIDE

Note: View is for a 12 pin package. All dimensions in the tables apply for the 16 pin package

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	1.35	1.50	1.65	
E2	1.35	1.50	1.65	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3		0.20 REF.		
D		3.00 BSC		
D1		2.75 BSC		
E		3.00 BSC		
E1		2.75 BSC		
θ			12°	
P	0.24	0.42	0.60	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

DISCLAIMER

Information in this document is provided in connection with Mindspeed Technologies™ ("Mindspeed™") products. These materials are provided by Mindspeed as a service to its customers and may be used for informational purposes only. Except as provided in Mindspeed's Terms and Conditions of Sale for such products or in any separate agreement related to this document, Mindspeed assumes no liability whatsoever. Mindspeed assumes no responsibility for errors or omissions in these materials. Mindspeed may make changes to specifications and product descriptions at any time, without notice. Mindspeed makes no commitment to update the information and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to its specifications and product descriptions. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document.

THESE MATERIALS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, RELATING TO SALE AND/OR USE OF MINDSPEED PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, CONSEQUENTIAL OR INCIDENTAL DAMAGES, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. MINDSPEED FURTHER DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. MINDSPEED SHALL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS, WHICH MAY RESULT FROM THE USE OF THESE MATERIALS.

Mindspeed products are not intended for use in medical, life saving or life sustaining applications. Mindspeed customers using or selling Mindspeed products for use in such applications do so at their own risk and agree to fully indemnify Mindspeed for any damages resulting from such improper use or sale.

Headquarters

Newport Beach
Mindspeed Technologies
4000 MacArthur Boulevard, East Tower
Newport Beach, CA 92660
Phone: (949) 579-3000
Fax: (949) 579-3020

MINDSPEED

www.mindspeed.com