

ACS139MS

Radiation Hardened Dual 2-to-4 Line Decoder/Demultiplexer

November 1997

Features

- · QML Qualified Per MIL-PRF-38535 Requirements
- 1.25Micron Radiation Hardened SOS CMOS
- Radiation Environment
 - Latch-up Free Under any Conditions
 - Total Dose 3 x 10⁵ RAD(Si)

 - SEU LET Threshold>100MeV/(mg/cm²)
- Input Logic Levels . . . $V_{IL} = (0.3)(V_{CC}), V_{IH} = (0.7)(V_{CC})$
- Quiescent Supply Current......400µA
- · Propagation Delay

Applications

- **Memory Decoding**
- Data Routing
- Code conversion

Description

The Radiation Hardened ACS139MS contains two independent binary to one-of-four decoders, each with a single active low enable input. Data on the select inputs cause one of the four normally high outputs to go low.

If the enable input is high, all four outputs remain high. During demultiplexer operation the enable input acts as the data input. The enable input also functions as a chip select when the devices are cascaded.

The ACS139MS is fabricated on a CMOS Silicon on Sapphire (SOS) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment. These devices offer significant power reduction and faster performance when compared to ALSTTL types.

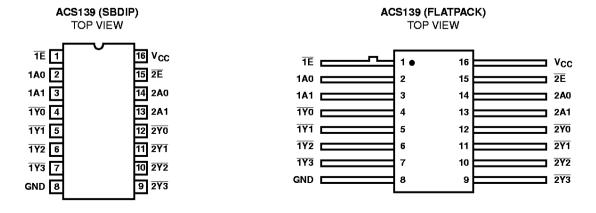
Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACS139 are contained in SMD 5962-97639. A "hot-link" is provided on our homepage with instructions for downloading. http://www.semi.harris.com/data/sm/index.htm

Ordering Information

SMD PART NUMBER	HARRIS PART NUMBER	TEMP. RANGE (^O C)	PACKAGE	CASE OUTLINE
5962F9763901VEC	ACS139DMSR-02	-55 to 125	16 Ld SBDIP	CDIP2-T16
N/A	ACS139D/Sample-02	25	16 Ld SBDIP	CDIP2-T16
5962F9763901VXC	ACS139KMSR-02	-55 to 125	16 Ld Flatpack	CDFP4-F16
N/A	ACS139K/Sample-02	25	16 Ld Flatpack	CDFP4-F16
N/A	ACS139HMSR-02	25	Die	N/A

Pinouts



ACS139MS

Die Characteristics

DIE DIMENSIONS:

Size: 2390μm x 2390μm (94 mils x 94 mils) Thickness: 525μm ±25μm (20.6 mils ±1 mil) Bond Pad: 110μm x 110μm (4.3 mils x 4.3 mils)

METALLIZATION:

Type: Al

Metal 1 Thickness: $0.7\mu m \pm 0.1\mu m$ Metal 2 Thickness: $1.0\mu m \pm 0.1\mu m$

SUBSTRATE:

Silicon on Sapphire (SOS)

SUBSTRATE POTENTIAL:

Unbiased Insulator

BACKSIDE FINISH:

Sapphire

PASSIVATION

Type: Phosphorous Silicon Glass (PSG)

Thickness: $1.30\mu m \pm 0.15\mu m$

SPECIAL INSTRUCTIONS:

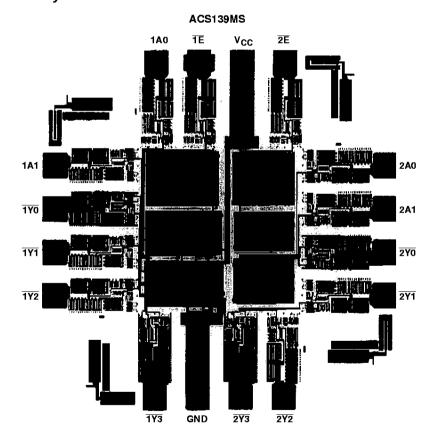
Bond V_{CC} First

ADDITIONAL INFORMATION:

Worst Case Density: <2.0 x 10⁵ A/cm²

Transistor Count: 190

Metallization Mask Layout



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