ML65F16241

16-Bit Buffer/Line Driver with 3-State Outputs

GENERAL DESCRIPTION

The ML65F16241 is a BiCMOS, 16-bit buffer/line driver with 3-state outputs. This device was specifically designed for high speed bus applications. Its 16 channels support propagation delay of 2ns maximum, and fast output enable and disable times of 5ns or less to minimize datapath delay.

This device is designed to minimize undershoot, overshoot, and ground bounce to decrease noise delays. These transceivers implement a unique digital and analog implementation to eliminate the delays and noise inherent in traditional digital designs. The device offers a new method for quickly charging up a bus load capacitor to minimize bus settling times, or FastBus™ Charge. FastBus Charge is a transition current, (specified as $I_{DYNAMIC}$) that injects between 60 to 200mA (depending on output load) of current during the rise time and fall time. This current is used to reduce the amount of time it takes to charge up a heavily-capacitive loaded bus, effectively reducing the bus settling times, and improving data/clock margins in tight timing budgets.

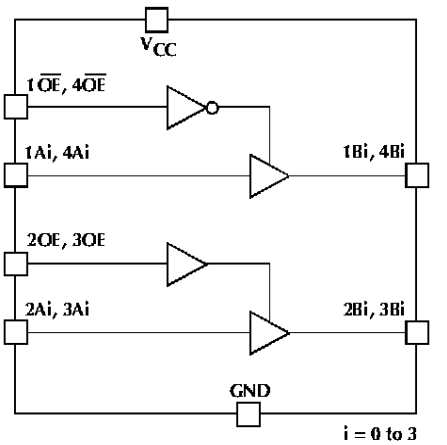
Micro Linear's solution is intended for applications for critical bus timing designs that include minimizing device propagation delay, bus settling time, and time delays due to noise. Applications include; high speed memory arrays, bus or backplane isolation, bus to bus bridging, and sub-2ns propagation delay schemes.

The ML65F16241 follows the pinout and functionality of the industry standard 2.7V to 3.6V-logic families.

FEATURES

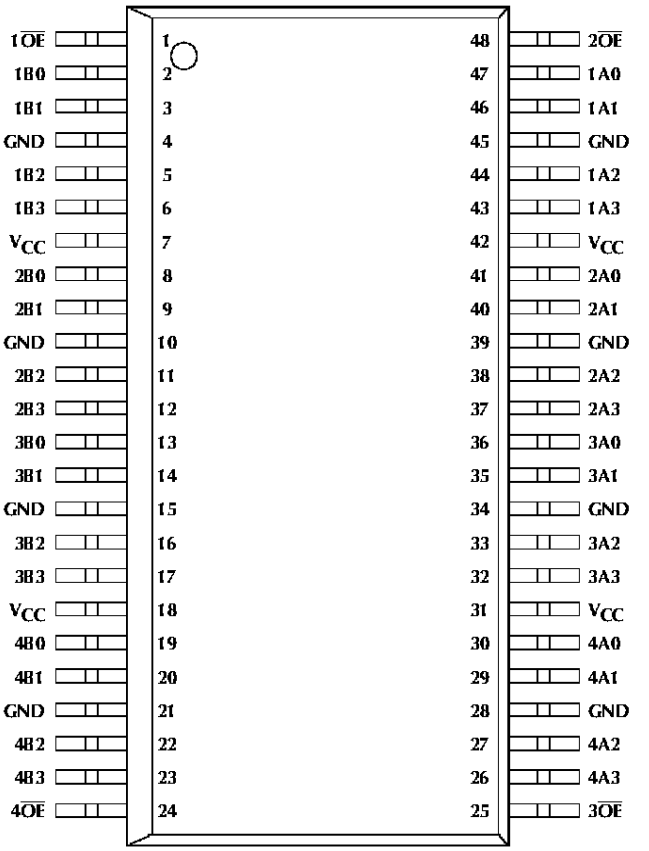
- Low propagation delays — 2ns maximum for 3.3V, 2.5ns maximum for 2.7V
- Fast output enable/disable times of 5ns maximum
- FastBus Charge current to minimize the bus settling time during active capacitive loading
- 2.7V to 3.6V V_{CC} supply operation; LV-TTL compatible input and output levels with 3-state capability
- Industry standard pinout compatible to FCT, ALV, LCX, LVT, and other low voltage logic families
- ESD protection exceeds 2000V
- Full output swing for increased noise margin
- Undershoot and overshoot protection to 400mV typically
- Low ground bounce design

BLOCK DIAGRAM



PIN CONFIGURATION

ML65F16241
48-Pin SSOP (R48)
48-Pin TSSOP (T48)



TOP VIEW

FUNCTION TABLE

(Each 4-bit section)

INPUTS		OUTPUTS
1$\overline{OE}$, 4$\overline{OE}$	1Ai, 4Ai	1Bi, 4Bi
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUTS
2OE, 3OE	2Ai, 3Ai	2Bi, 3Bi
H	H	H
H	L	L
L	X	Z

L = Logic Low, H = Logic High, X = Don't Care, Z = High Impedance

i = 0 to 3

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$1\overline{OE}$	Output Enable Active Low
2	1B0	Data Output
3	1B1	Data Output
4	GND	Signal Ground
5	1B2	Data Output
6	1B3	Data Output
7	V_{CC}	2.7V to 3.6V Supply
8	2B0	Data Output
9	2B1	Data Output
10	GND	Signal Ground
11	2B2	Data Output
12	2B3	Data Output
13	3B0	Data Output
14	3B1	Data Output
15	GND	Signal Ground
16	3B2	Data Output
17	3B3	Data Output
18	V_{CC}	2.7V to 3.6V Supply
19	4B0	Data Output
20	4B1	Data Output
21	GND	Signal Ground
22	4B2	Data Output
23	4B3	Data Output
24	$4\overline{OE}$	Output Enable Active Low

PIN	NAME	FUNCTION
25	3OE	Output Enable Active High
26	4A3	Data Input
27	4A2	Data Input
28	GND	Signal Ground
29	4A1	Data Input
30	4A0	Data Input
31	V_{CC}	2.7V to 3.6V Supply
32	3A3	Data Input
33	3A2	Data Input
34	GND	Signal Ground
35	3A1	Data Input
36	3A0	Data Input
37	2A3	Data Input
38	2A2	Data Input
39	GND	Signal Ground
40	2A1	Data Input
41	2A0	Data Input
42	V_{CC}	2.7V to 3.6V Supply
43	1A3	Data Input
44	1A2	Data Input
45	GND	Signal Ground
46	1A1	Data Input
47	1A0	Data Input
48	2OE	Output Enable Active High

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} 7V
DC Input Voltage ..... –0.3V to V_{CC} + 0.3V
AC Input Voltage (PW < 20ns) ..... –3.0V
DC Output Voltage ..... –0.3V to 7VDC
Output Current, Source or Sink (AC) 180mA

Storage Temperature Range ..... –65°C to 150°C
Junction Temperature ..... 150°C
Lead Temperature (Soldering, 10sec) ..... 150°C
Thermal Impedance (θ_{JA}) ..... 76°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
V_{IN} Operating Range ..... 2.7V to 3.6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 3.3V, T_A = Operating Temperature Range (Note 1).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF)							
t_{PHL}, t_{PLH}	Propagation Delay	Ai to Bi	3.3V	1.35	1.7	2	ns
			2.7V	1.25	1.9	2.5	ns
t_{OE}	Output Enable Time	OE to Ai/Bi	3.3V			5	ns
			2.7V			6	ns
		DIR to Ai/Bi	3.3V			5	ns
			2.7V			6	ns
t_{OD}	Output Disable Time	OE to Ai/Bi	3.3V			5	ns
			2.7V			6	ns
		DIR to Ai/Bi	3.3V			5	ns
			2.7V			6	ns
T_{OS}	Output-to-Output Skew					300	ps
C_{IN}	Input Capacitance					5	pF
DC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = Open)							
V_{IH}	Input High Voltage	Logic high		2.0			V
V_{IL}	Input Low Voltage	Logic low				0.8	V
I_{IH}	Input High Current	Per pin, V_{IN} = 3V				300	mA
I_{IL}	Input Low Current	Per pin, V_{IN} = 0V				300	mA
I_{HI-Z}	Three-State Output Current	V_{CC} = 3.6V, 0 < V_{IN} < V_{CC}				5	mA
V_{IC}	Input Clamp Voltage	V_{CC} = 3.6V, I_{IN} = 18mA			–0.7	–0.2	V
$I_{DYNAMIC}$	Dynamic Transition Current (FastBus Charge)	Low to high transitions			80		mA
		High to low transitions			80		mA
V_{OH}	Output High Voltage		V_{CC} = 3.6V	2.4	3.4		V
			V_{CC} = 2.7V	2.25	2.35		V
V_{OL}	Output LowVoltage	V_{CC} = 2.7V and 3.6V				0.6	V
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, f = 0Hz, Inputs = V_{CC} or 0V				3	µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

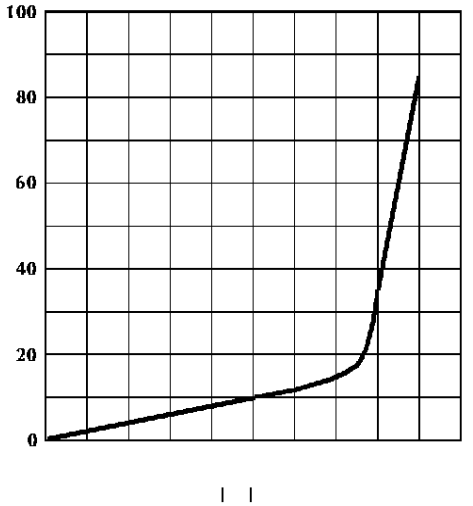


Figure 1a. Typical V_{OL} vs. I_{OL} for 3.3V V_{CC}. One Buffer Output

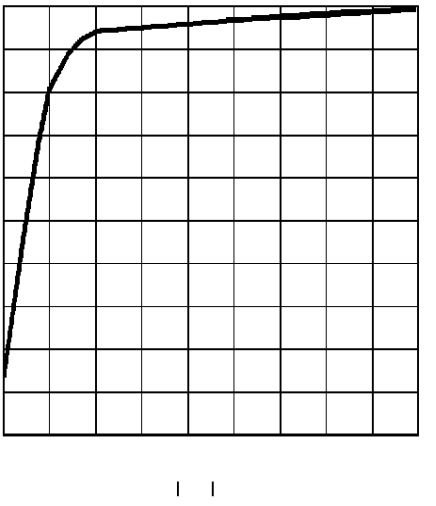


Figure 1b. Typical V_{OH} vs. I_{OH} for 3.3V V_{CC}. One Buffer Output

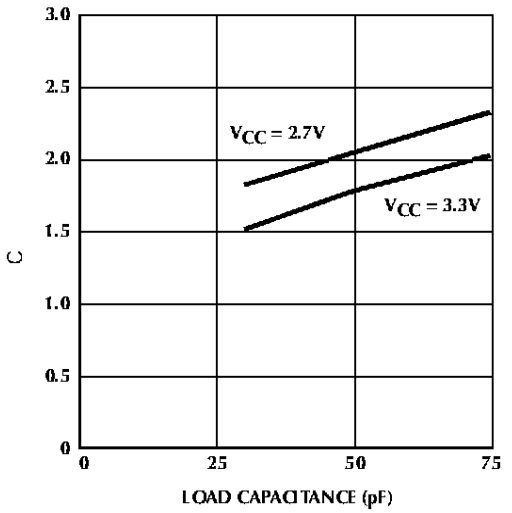


Figure 2a. Propagation Delay vs. Load Capacitance: 3.3V, 50MHZ

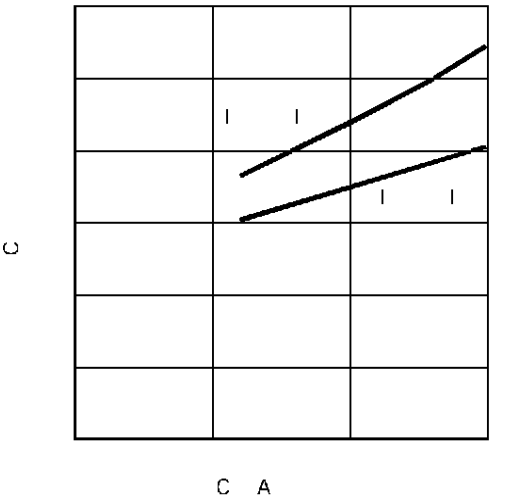


Figure 2b. Propagation Delay vs. Load Capacitance: 2.7V, 50MHZ

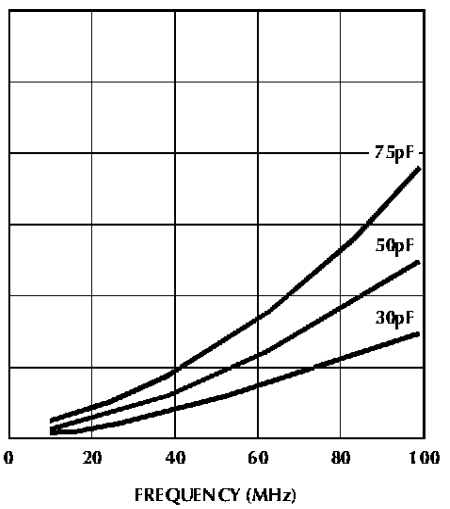


Figure 3a. I_{CC} vs. Frequency: V_{CC} = V_{IN} = 3.3V. One Buffer Output

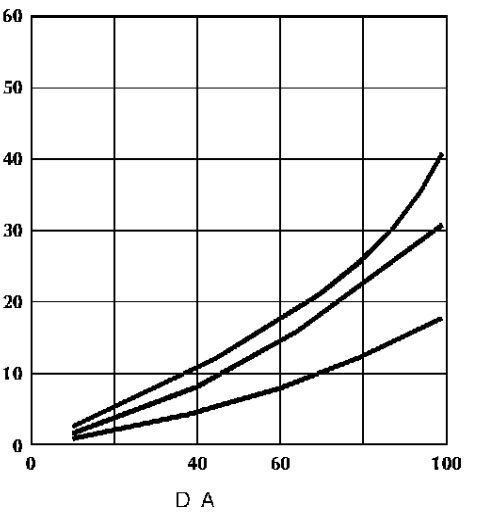


Figure 3b. I_{CC} vs. Frequency: V_{CC} = V_{IN} = 2.7V. One Buffer Output

FUNCTIONAL DESCRIPTION

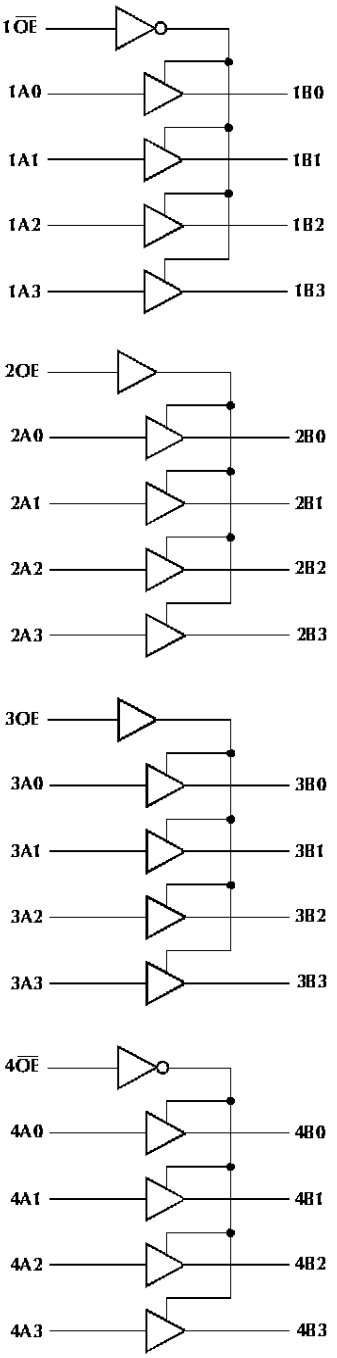


Figure 4. Logic Diagram

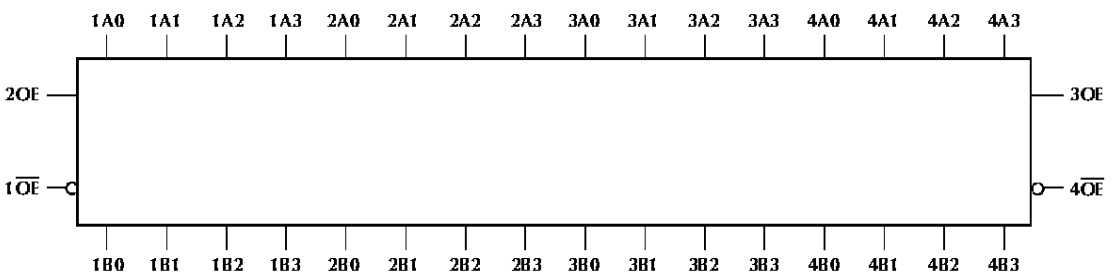


Figure 5. Logic Symbol

ARCHITECTURAL DESCRIPTION

The ML65F16241 is a 16-bit buffer/line driver with 3-state outputs designed for 2.7V to 3.6V V_{CC} operation. This device is designed for Quad-Nibble, Dual-Byte memory interleaving operations. Each bank has an independently controlled 3-state output enable pin with output enable/ disable access times of less than 7ns. Each bank is configured to have four independent buffer/line drivers. Two banks are active high enabled and the other two banks are active low enabled. Thus making this device ideal for nibble or byte swapping operations in cache or main memory designs by toggling between the active low and active high output enable pins.

Until now, these transceivers were typically implemented in CMOS logic and made to be TTL compatible by sizing the input devices appropriately. In order to buffer large capacitances with CMOS logic, it is necessary to cascade an even number of inverters, each successive inverter larger than the preceding, eventually leading to an inverter that will drive the required load capacitance at the required frequency. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. The best of these 16-bit CMOS buffers has managed to drive 50pF load capacitance with a delay of 3ns.

Micro Linear has produced a 16-bit buffer/line driver with a delay less than 2ns (3.3V) by using a unique circuit architecture that does not require cascade logic gates.

The basic architecture of the ML65F16241 is shown in Figure 6. In this circuit, there are two paths to the output. One path sources current to the load capacitance where the signal is asserted, and the other path sinks current from the output when the signal is negated.

The assertion path is the Darlington pair consisting of transistors Q1 and Q2. The effect of transistor Q1 is to increase the current gain through the stage from input to output, to increase the input resistance and to reduce input capacitance. During an input low-to-high transition, the output transistor Q2 sources large amount of current to quickly charge up a highly capacitive load which in effect reduces the bus settling time. This current is specified as $I_{DYNAMIC}$.

The negation path is also the Darlington pair consisting of transistor Q3 and transistor Q4. With M1 connecting to the input of the Darlington pair, Transistor Q4 then sinks a large amount of current during the input transition from high-to-low.

Inverter X2 is a helpful buffer that not only drives the output toward the upper rail but also pulls the output to the lower rail.

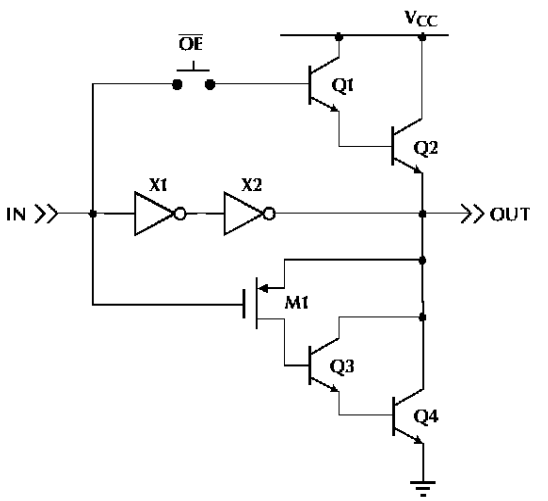


Figure 6. One Buffer Cell of the ML65F16241

CIRCUITS AND WAVE FORMS

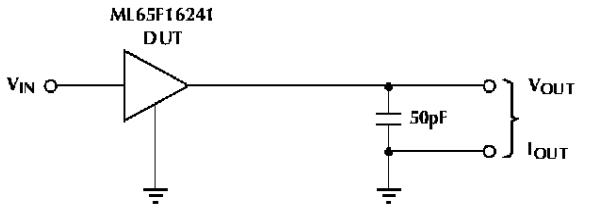


Figure 7. Test Circuits for All Outputs

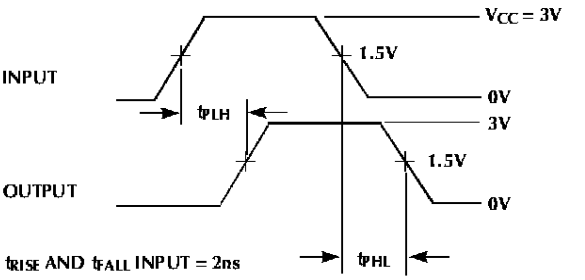


Figure 8. Propagation Delay

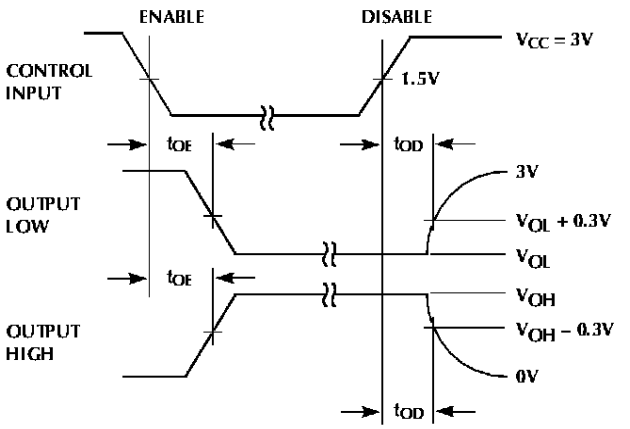


Figure 9. Enable and Disable Times

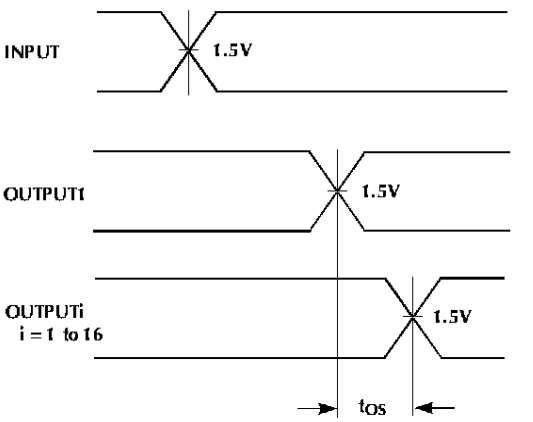
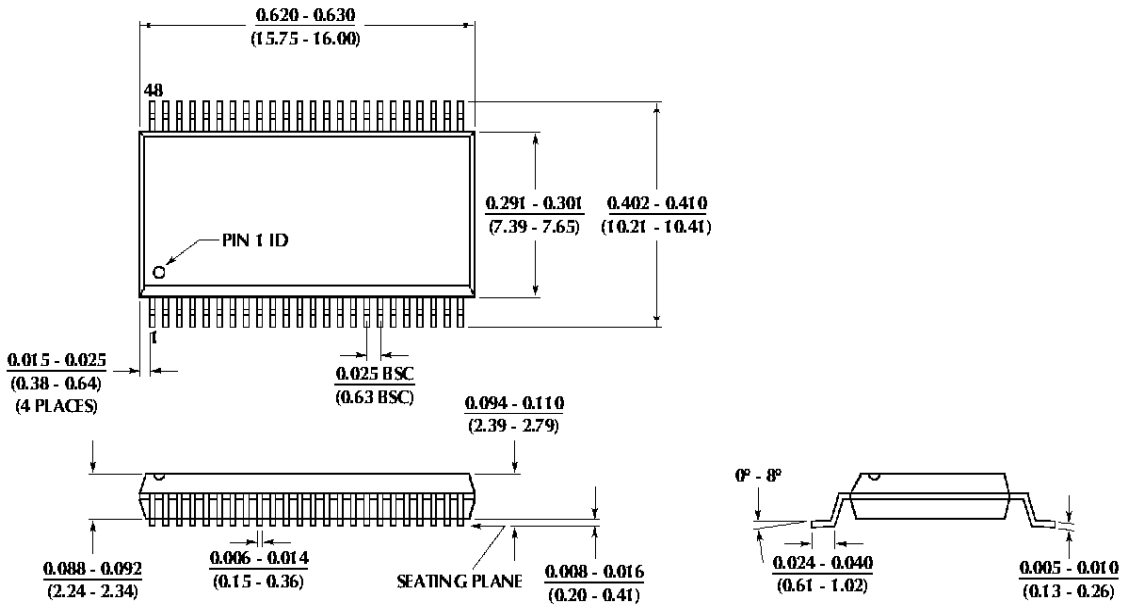


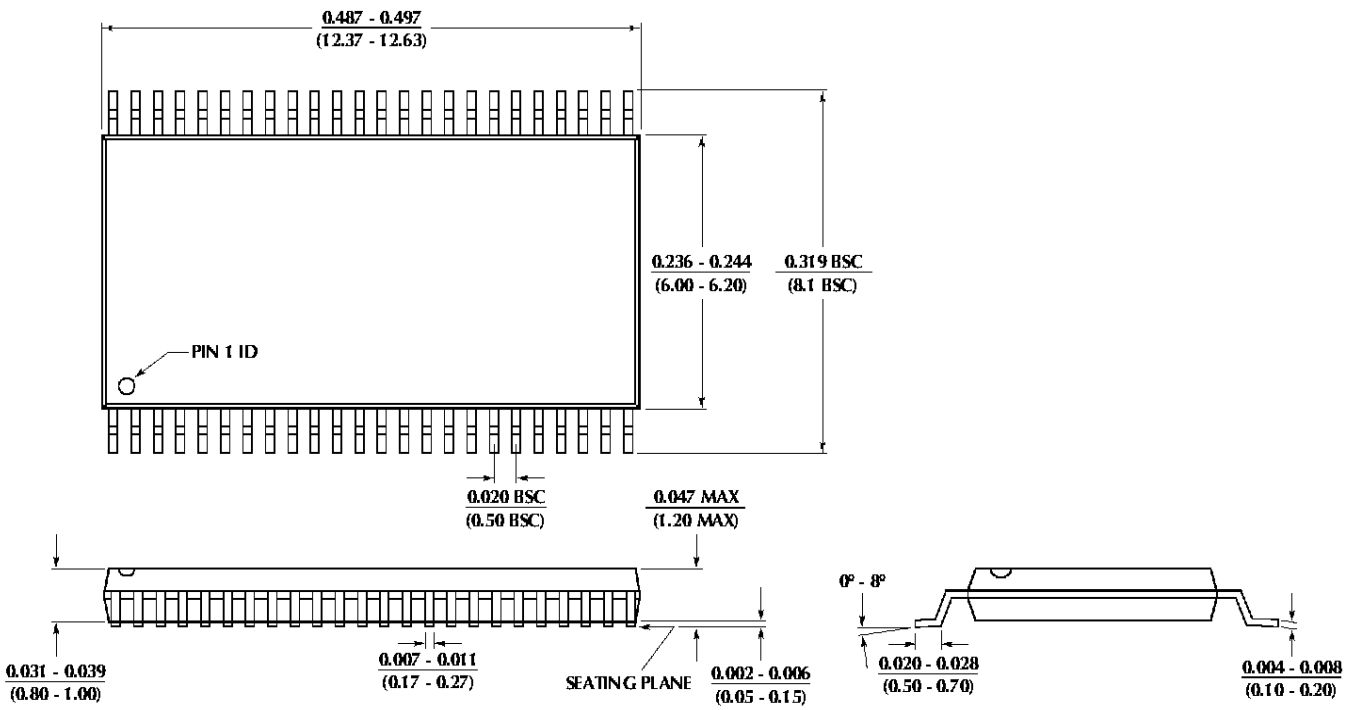
Figure 10. Output Skew

PHYSICAL DIMENSIONS inches (millimeters)

Package: R48
48-Pin SSOP



Package: T48
48-Pin TSSOP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML65F16241CR	0°C to 70°C	48-Pin SSOP (R48)
ML65F16241CT	0°C to 70°C	48-Pin TSSOP (T48)

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