



# 3.3V CMOS 32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

**IDT74LVCH32373A**

## FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.8mm pitch LFBGA package, 96 balls
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

## Drive Features for LVCH32373A:

- Balanced Output Drivers: ±24mA
- Reduced system switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

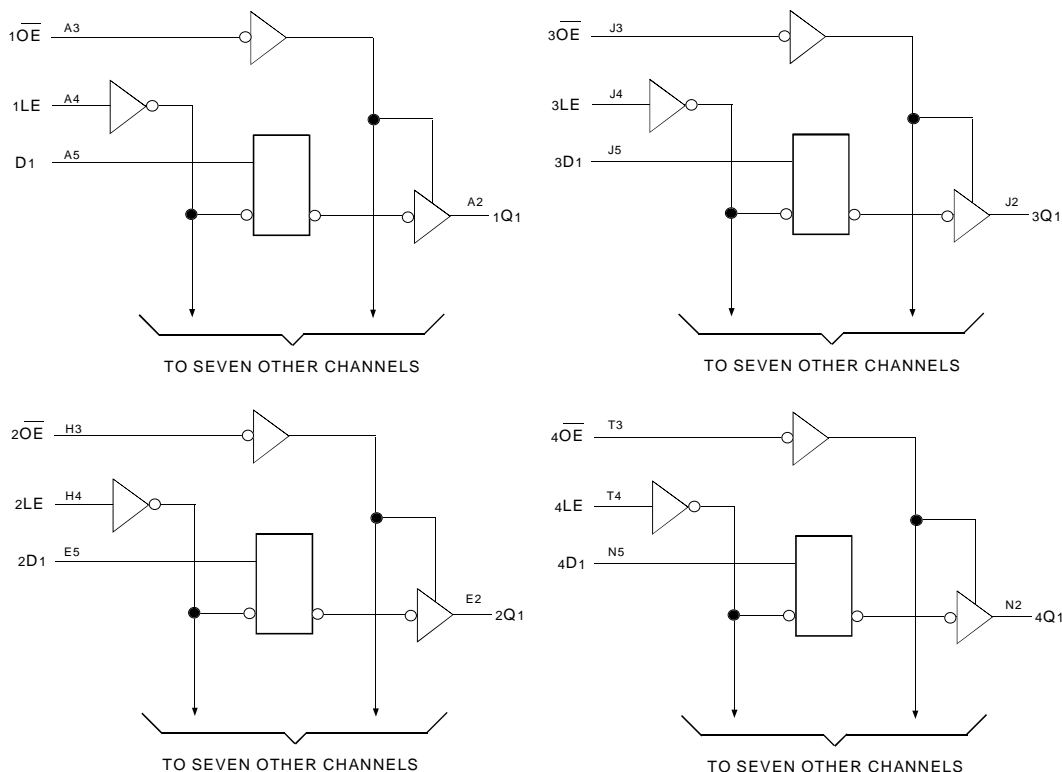
The LVCH32373A 32-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. The device can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as four 8-bit latches, two 16-bit latches, or one 32-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of the LVCH32373A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH32373A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH32373A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



**EXTENDED COMMERCIAL TEMPERATURE RANGE**

**JANUARY 2000**

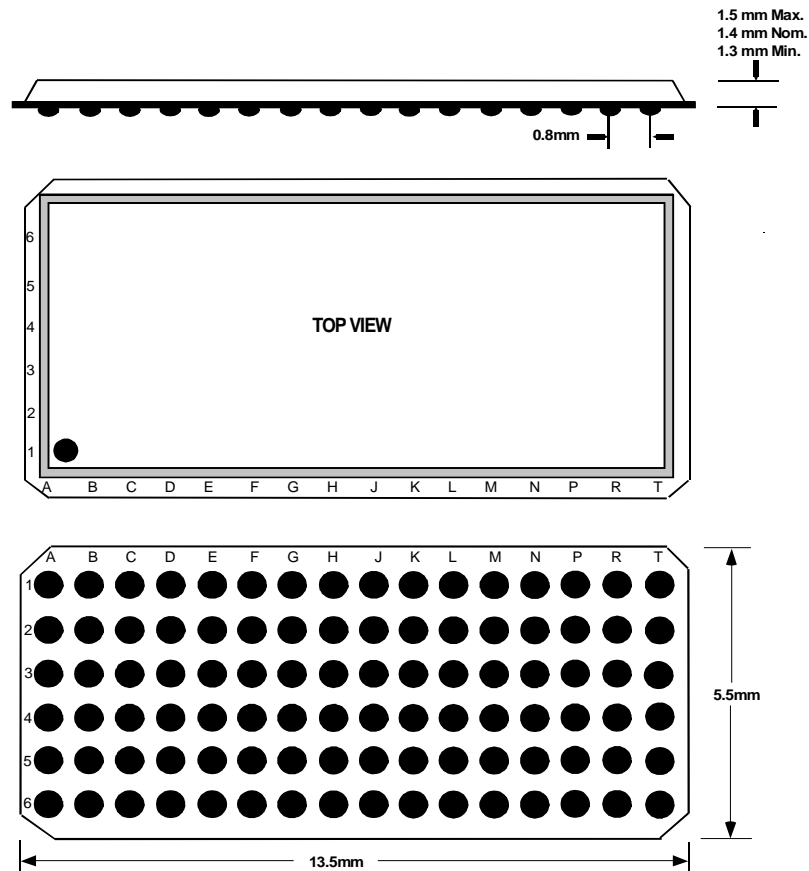
### PIN CONFIGURATION

6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1LE	GND	VCC	GND	GND	VCC	GND	2LE	3LE	GND	VCC	GND	GND	VCC	GND	4LE
3	1OE	GND	VCC	GND	GND	VCC	GND	2OE	3OE	GND	VCC	GND	GND	VCC	GND	4OE
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

32373

### LFBGA TOP VIEW

### 96 BALL LFBGA PACKAGE LAYOUT



**ABSOLUTE MAXIMUM RATINGS (1)**

Symbol	Description	Max.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
T <sub>STG</sub>	Storage Temperature	- 65 to +150	°C
I <sub>OUT</sub>	DC Output Current	- 50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	± 100	mA

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**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)**

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

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**NOTE:**

1. As applicable to the device type.

**BUS-HOLD CHARACTERISTICS**

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I <sub>BHH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3.0V	V <sub>I</sub> = 2.0V	- 75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
I <sub>BHH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	—	—	—	μA
			V <sub>I</sub> = 0.7V	—	—	—	
I <sub>BHHO</sub> I <sub>BHLO</sub>	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	± 500	μA

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**NOTES:**

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

**PIN DESCRIPTION**

Pin Names	Description
xDx	Data Inputs <sup>(1)</sup>
xLE	Latch Enable Inputs (Active HIGH)
x $\overline{OE}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

**NOTE:**

1. These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

**FUNCTION TABLE (EACH 9-BIT SECTION) (1)**

Inputs			Outputs
xDx	xLE	x $\overline{OE}$	xQx
H	H	L	H
L	H	L	L
X	X	H	Z
X	L	L	Q <sub>0</sub>

**NOTE:**

1. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
Q<sub>0</sub> = Output level of Q before the indicated steady-state conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub> I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 5.5V	—	—	±5	μA
IOZH IOZL	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = 0 to 5.5V	—	—	±10	μA
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 5.5V		—	—	±50	μA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CCL</sub> I <sub>CCH</sub> I <sub>CCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V	V <sub>IN</sub> = GND or V <sub>CC</sub>	—	—	10	μA
			3.6 ≤ V <sub>IN</sub> ≤ 5.5V <sup>(2)</sup>	—	—	10	
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V other inputs at V <sub>CC</sub> or GND		—	—	500	μA

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### NOTES:

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3.0V		2.4	—	
		V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = -24mA	2.2	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 24mA	—	0.55	

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### NOTE:

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = -40°C to +85°C.

**OPERATING CHARACTERISTICS,  $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 25^\circ C$**

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Latch Outputs enabled	CL = 0pF, f = 10Mhz	78	pF
CPD	Power Dissipation Capacitance per Latch Outputs disabled		12	pF

**SWITCHING CHARACTERISTICS (1)**

Symbol	Parameter	Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay xDx to xQx	1.5	4.9	1.6	4.2	ns
tPLH tPHL	Propagation Delay xLE to xQx	2	5.3	2.1	4.6	ns
tPZH tPZL	Output Enable Time xOE to xQx	1.5	5.7	1.3	4.7	ns
tPHZ tPLZ	Output Disable Time xOE to xQx	1.5	6.3	2.5	5.9	ns
tsu	Set-up Time HIGH or LOW, xDx to xLE	1.7	—	1.7	—	ns
th	Hold Time HIGH or LOW, xDx after xLE	1.2	—	1.2	—	ns
tw	xLE Pulse Width HIGH	3.3	—	3.3	—	ns
tsk(o)	Output Skew <sup>(2)</sup>	—	—	—	500	ns

**NOTES:**

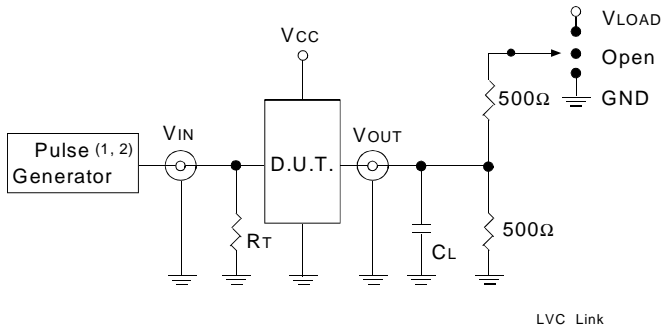
1. See test circuits and waveforms.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> (1) = 3.3V ± 0.3V	V <sub>CC</sub> (1) = 2.7V	V <sub>CC</sub> (2) = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

### TEST CIRCUITS FOR ALL OUTPUTS



#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

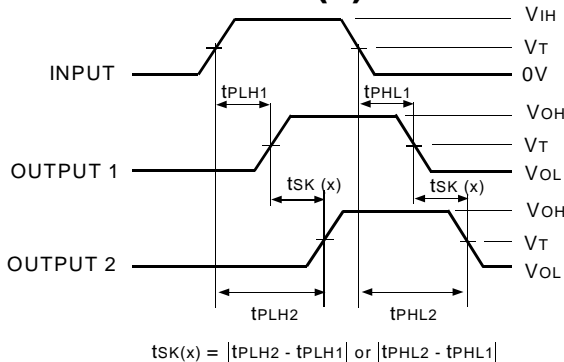
#### NOTES:

- Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
- Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

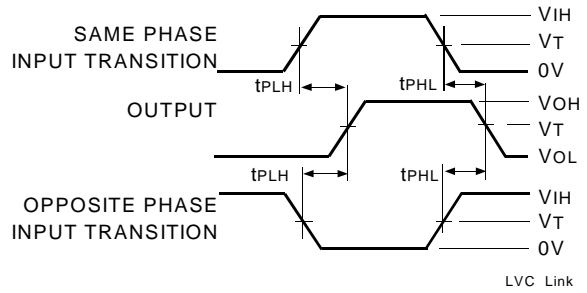
### OUTPUT SKEW - t<sub>SK</sub>(x)



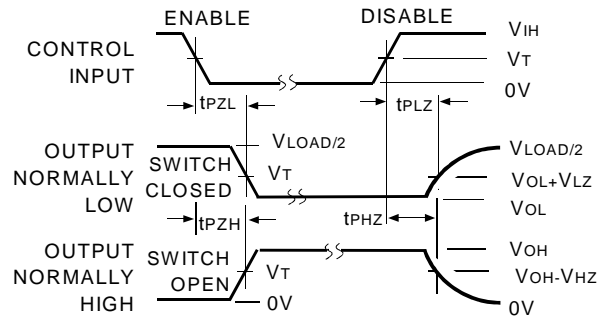
#### NOTES:

- For t<sub>SK</sub>(a) OUTPUT1 and OUTPUT2 are any two outputs.
- For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



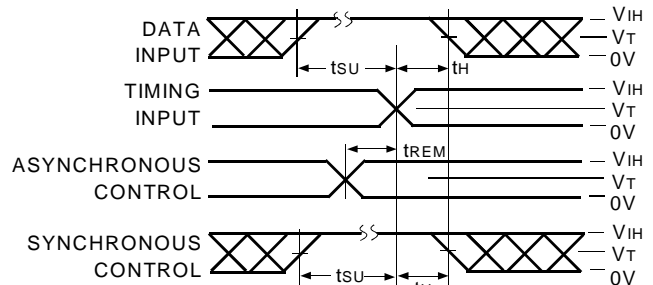
### ENABLE AND DISABLE TIMES



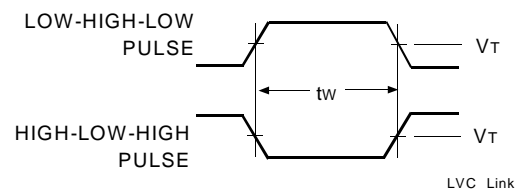
#### NOTE:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

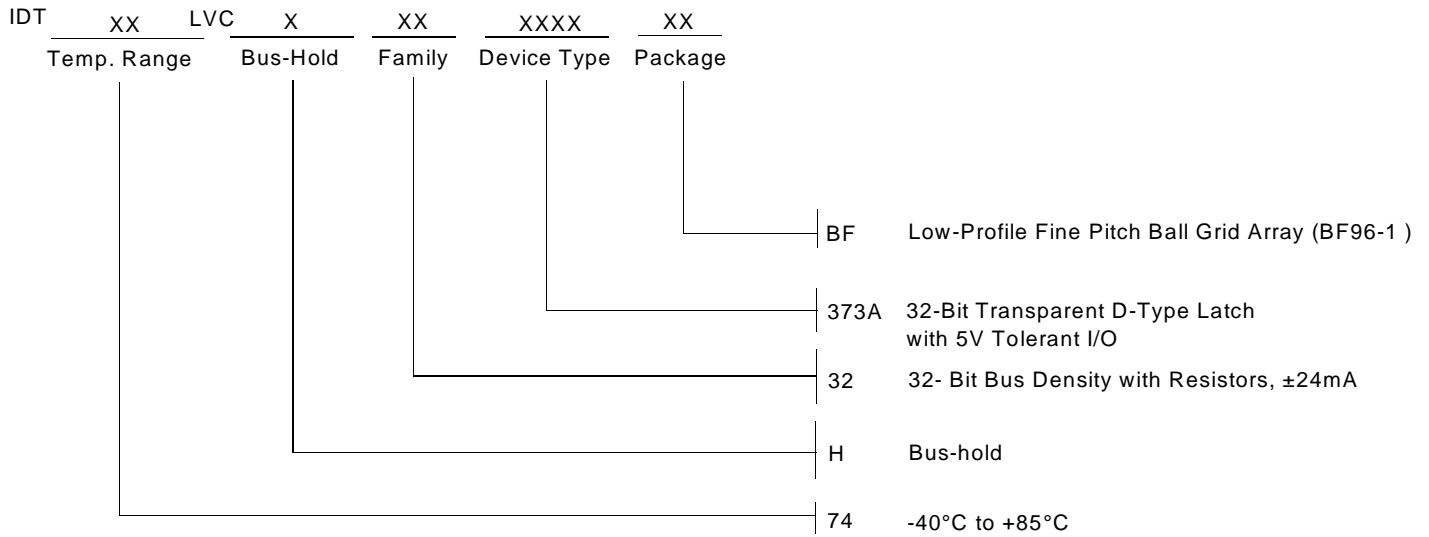
### SET-UP, HOLD, AND RELEASE TIMES



### PULSE WIDTH



## ORDERING INFORMATION



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