TC74HCT137AP/AF

3-TO-8 LINE DECODER/LATCH

The TC74HCT137A is a high speed CMOS 3-to-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

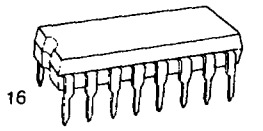
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

It is composed of a 3-bit input latches with a common $\overline{GL}$ enable input and a 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into the input latch on the high level of $\overline{GL}$. The value of this data determines which one of the outputs will go low. When the enable input G1 is held low or $\overline{G2}$ is held high, decoding function is inhibited and all the 8 outputs go high. The two enable inputs are provided to ease cascade connection and permits the application of address decoder for memory system.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=17ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IH} = 2V(Min.)
  V_{IL} = 0.8V(Max.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS137



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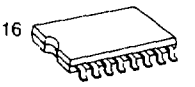

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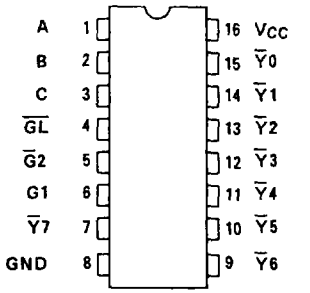
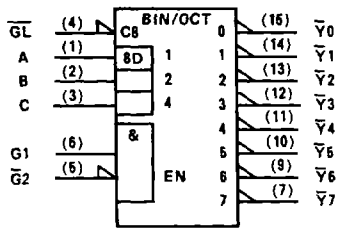
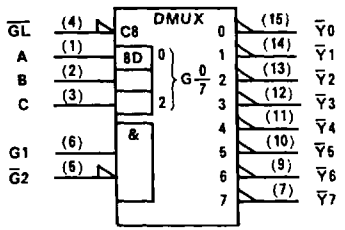
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



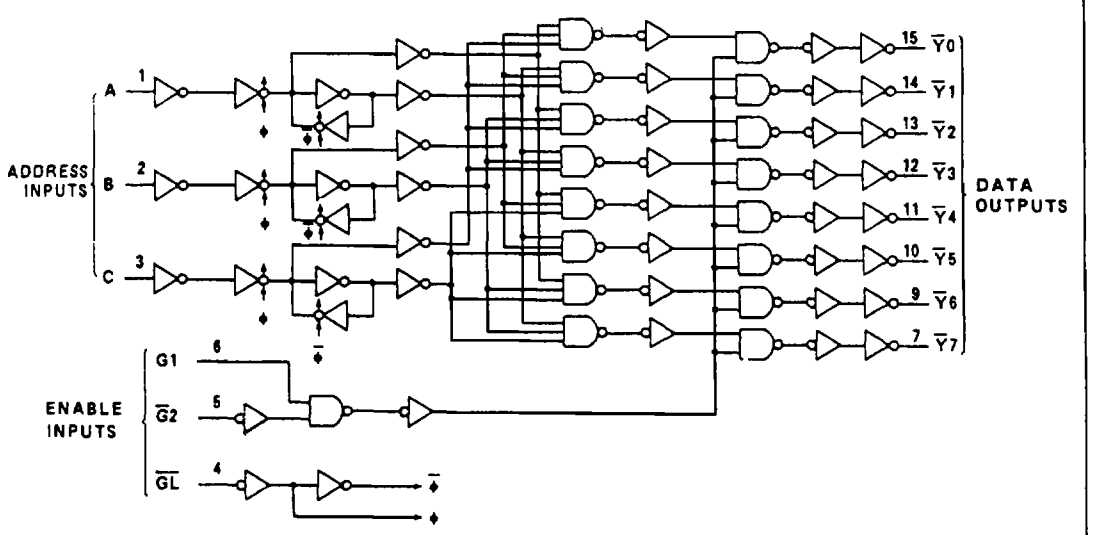


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			ADDRESS											
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
X	X	L	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
L	L	H	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
L	L	H	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
L	L	H	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
L	L	H	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
L	L	H	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
L	L	H	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
L	L	H	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
L	L	H	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$
H	L	H	X	X	X	OUTPUTS are latched at the time when $\overline{GL}$ is taken High level.								

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta=−40℃∼65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$4.5 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 500$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∼ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ∼ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
Low-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{OL}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	
Quiescent Supply Current	ΔI_{CC}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{GL}$)	$t_{W(L)}$		4.5	−	10	13	ns
			5.5	−	9	11	
Minimum Set-up Time (A, B, C−$\overline{GL}$)	t_s		4.5	−	10	13	
			5.5	−	9	11	
Minimum Hold Time (A, B, C−$\overline{GL}$)	t_h		4.5	−	5	5	
			5.5	−	5	5	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time ($G1 \cdot \overline{Y}$)	t_{pLH} t_{pHL}		−	15	23	
Propagation Delay Time ($\overline{G2} \cdot \overline{Y}$)	t_{pLH} t_{pHL}		−	15	23	
Propagation Delay Time ($\overline{GL}$−$\overline{Y}$)	t_{pLH} t_{pHL}		−	22	32	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pLH} t_{pHL}		−	21	32	

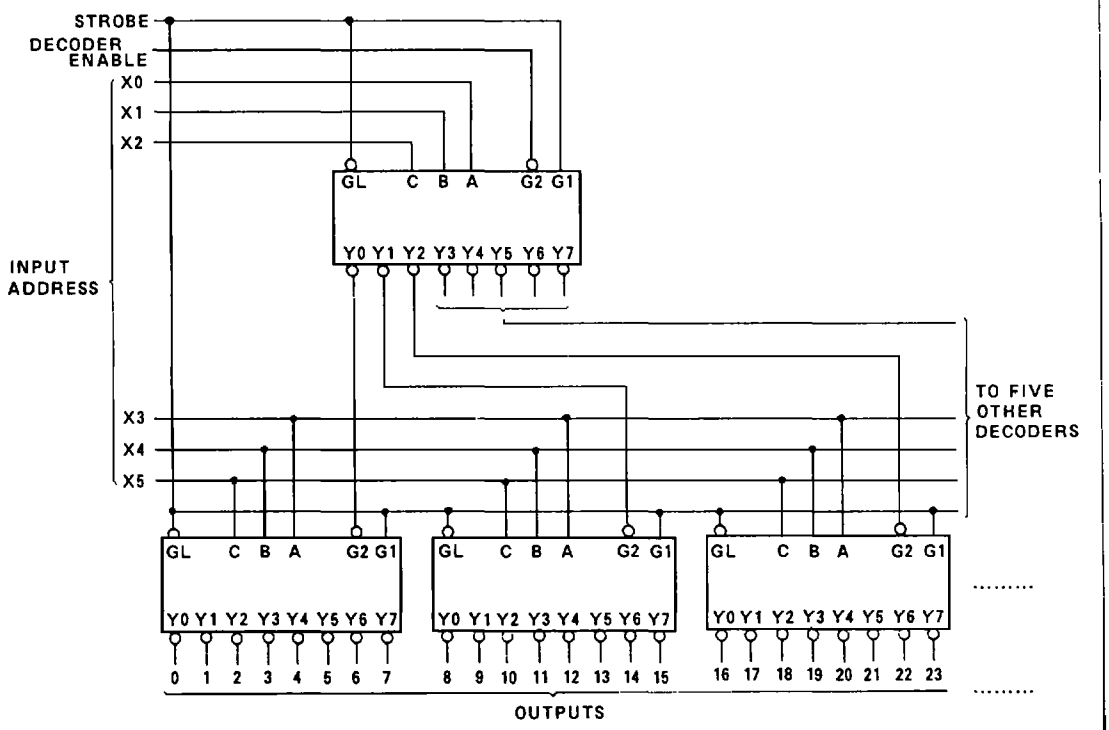
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	−	8	15	−	19	ns
			5.5	−	7	13	−	16	
Propagation Delay Time ($G1-\overline{Y}$)	t_{pLH} t_{pHL}		4.5	−	18	27	−	34	
			5.5	−	16	24	−	31	
Propagation Delay Time ($\overline{G2}-\overline{Y}$)	t_{pHL} t_{pHL}		4.5	−	19	29	−	36	
			5.5	−	17	26	−	33	
Propagation Delay Time ($\overline{GL}-\overline{Y}$)	t_{pHL} t_{pHL}		4.5	−	26	38	−	48	
			5.5	−	20	34	−	43	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pHL} t_{pHL}		4.5	−	25	38	−	48	
			5.5	−	23	34	−	43	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	56	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage