

HCTS240AMS

Radiation Hardened Octal Buffer/Line Driver, Three-State

FN2105
Rev 2.00
September 1995

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm²/mg
- Single Event Upset (SEU) Immunity < 2 x 10⁻⁹ Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10¹² RAD (Si)/s
- Dose Rate Upset >10¹⁰ RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
 - VIL = 0.8V Max
 - VIH = VCC/2 Min
- Input Current Levels $I_i \leq 5\mu\text{A}$ at VOL, VOH

Description

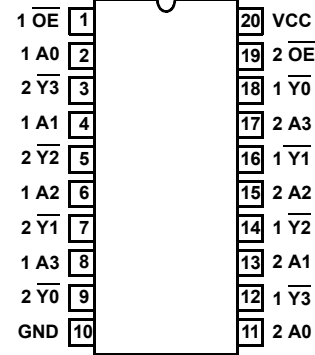
The Intersil HCTS240AMS is a Radiation Hardened inverting octal buffer/line driver, three-state, with two active low output enables (1OE, 2OE). 1OE controls outputs 1Yn, 2OE controls outputs 2Yn.

The HCTS240AMS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family .

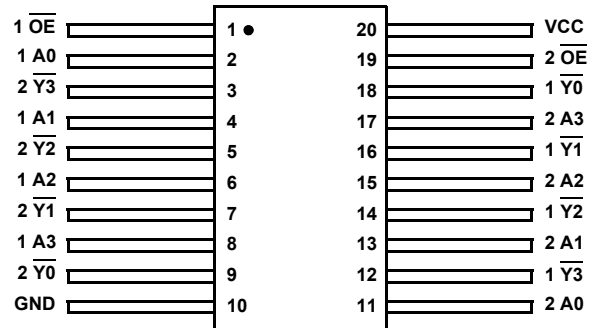
The HCTS240AMS is supplied in a 20 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T20, LEAD FINISH C
TOP VIEW



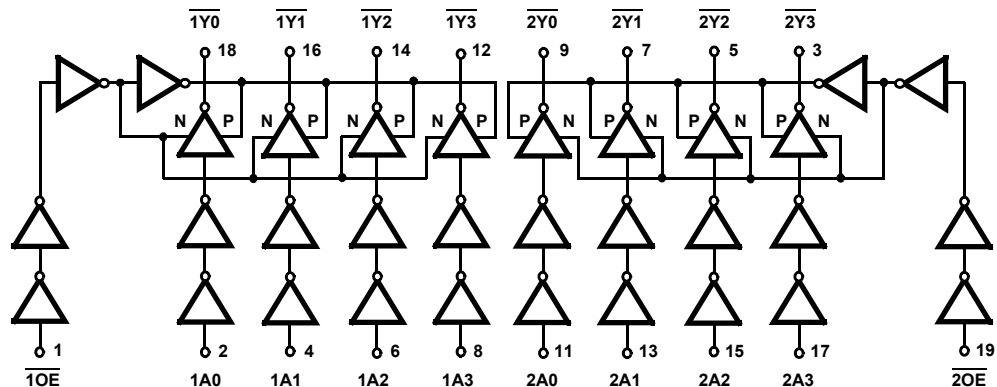
20 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F20, LEAD FINISH C
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCTS240ADMSR	-55°C to +125°C	Intersil Class S Equivalent	20 Lead SBDIP
HCTS240AKMSR	-55°C to +125°C	Intersil Class S Equivalent	20 Lead Ceramic Flatpack
HCTS240AD/Sample	+25°C	Sample	20 Lead SBDIP
HCTS240AK/Sample	+25°C	Sample	20 Lead Ceramic Flatpack
HCTS240AHMSR	+25°C	Die	Die

Functional Diagram



TRUTH TABLE

INPUTS		OUTPUT
$\overline{1OE}, \overline{2OE}$	A	Y
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
 L = Low Voltage Level
 X = Immaterial
 Z = High Impedance

Absolute Maximum Ratings

Supply Voltage (VCC)	-0.5V to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output (All Voltage Reference to the VSS Terminal)	±35mA
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	72°C/W	24°C/W
Ceramic Flatpack Package	107°C/W	28°C/W
Maximum Package Power Dissipation at +125°C Ambient		
SBDIP Package	0.69W	
Ceramic Flatpack Package	0.47W	
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:		
SBDIP Package	13.9mW/°C	
Ceramic Flatpack Package	9.3mW/°C	

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage	+4.5V to +5.5V	Input Low Voltage (VIL)	0.0V to 0.8V
Input Rise and Fall Times at 4.5V VCC (TR, TF)	100ns Max	Input High Voltage (VIH)	VCC to VCC/2V
Operating Temperature Range (TA)	-55°C to +125°C		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOU = 0.4V, VIL = 0V, (Note 2)	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOU = VCC - 0.4V, VIL = 0V, (Note 2)	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Applied Voltage = 0V or VCC	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	V

NOTES:

- All voltages referenced to device GND.
- Force/measure functions may be interchanged.
- For functional tests, $VO \geq 4.0V$ is recognized as a logic "1", and $VO \leq 0.5V$ is recognized as a logic "0".
- Due to tester noise at -55°C VIH is increased 200mV.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Input to Output	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	23	ns
Propagation Delay Enable to Output	TPZL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	35	ns
	TPZH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns
Propagation Delay Disable to Output	TPLZ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	26	ns
	TPHZ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	23	ns

NOTES:

- All voltages referenced to device GND.
- AC measurements assume $R_L = 500\Omega$, $C_L = 50\text{pF}$, Input $t_r = t_f = 3\text{ns}$, $V_{IL} = \text{GND}$, $V_{IH} = 3\text{V}$.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	+25°C	-	135	pF
			+125°C, -55°C		150	pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	+25°C	-	10	pF
			+125°C, -55°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	+25°C	-	20	pF
			+125°C, -55°C	-	20	pF

NOTE:

- The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V	+25°C	6.0	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	+25°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOL = 50 μ A	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOL = 50 μ A	+25°C	-	0.1	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOH = -50 μ A	+25 $^{\circ}$ C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOH = -50 μ A	+25 $^{\circ}$ C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25 $^{\circ}$ C	-	\pm 5	μ A
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25 $^{\circ}$ C	-	\pm 50	μ A
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, (Note 2)	+25 $^{\circ}$ C	-	-	V
Propagation Delay Input to Output	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25 $^{\circ}$ C	2	25	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25 $^{\circ}$ C	2	23	ns
Propagation Delay Enable to Output	TPZL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25 $^{\circ}$ C	2	35	ns
	TPZH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25 $^{\circ}$ C	2	25	ns
Propagation Delay Disable to Output	TPLZ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25 $^{\circ}$ C	2	26	ns
	TPHZ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25 $^{\circ}$ C	2	23	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests $VO \geq 4.0V$ is recognized as a logic "1", and $VO \leq 0.5V$ is recognized as a logic "0".

TABLE 5. DELTA PARAMETERS (+25 $^{\circ}$ C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12 μ A
IOZ	5	\pm 200nA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA	100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA	100%/5004	1, 7, 9, Deltas	
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	1, 7, 9	
Group D	Sample/5005	1, 7, 9	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
--------------------	--------	-------------------	-----------------

NOTE:

1. Alternate group A inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	10	-	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	2, 4, 6, 8, 11, 13, 15, 17	-

NOTES:

1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

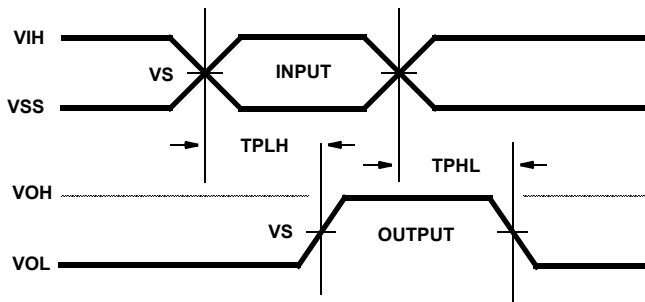
Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)	100% Interim Electrical Test 1 (T1)
GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects	100% Delta Calculation (T0-T1)
100% Nondestructive Bond Pull, Method 2023	100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015
Sample - Wire Bond Pull Monitor, Method 2011	100% Interim Electrical Test 2 (T2)
Sample - Die Shear Monitor, Method 2019 or 2027	100% Delta Calculation (T0-T2)
100% Internal Visual Inspection, Method 2010, Condition A	100% PDA 1, Method 5004 (Notes 1 and 2)
100% Temperature Cycle, Method 1010, Condition C, 10 Cycles	100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015
100% Constant Acceleration, Method 2001, Condition per Method 5004	100% Interim Electrical Test 3 (T3)
100% PIND, Method 2020, Condition A	100% Delta Calculation (T0-T3)
100% External Visual	100% PDA 2, Method 5004 (Note 2)
100% Serialization	100% Final Electrical Test
100% Initial Electrical Test (T0)	100% Fine/Gross Leak, Method 1014
100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015	100% Radiographic, Method 2012 (Note 3)
	100% External Visual, Method 2009
	Sample - Group A, Method 5005 (Note 4)
	100% Data Package Generation (Note 5)

NOTES:

- Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
- Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
- Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
- Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
- Data Package Contents:
 - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
 - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
 - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
 - X-Ray report and film. Includes penetrometer measurements.
 - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
 - Lot Serial Number Sheet (Good units serial number and lot number).
 - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
 - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

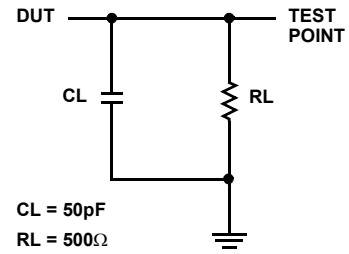
Propagation Delay Timing Diagrams



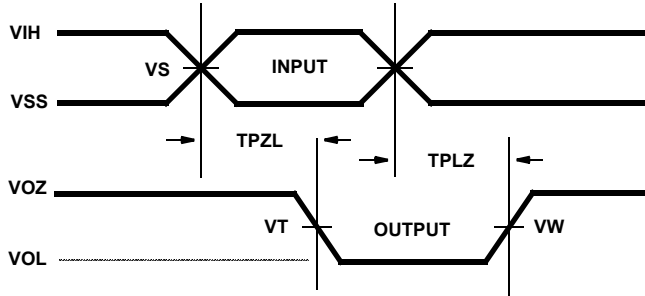
VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Propagation Delay Load Circuit



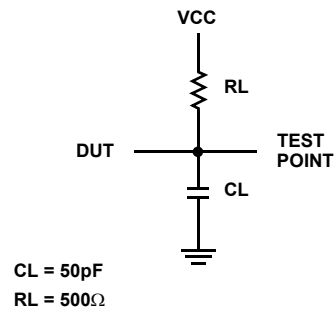
Three-State Low Timing Diagrams



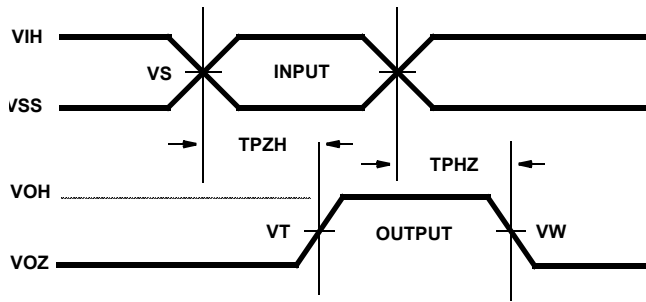
THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

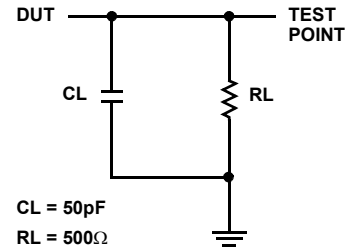
Three-State Low Load Circuit



Three-State High Timing Diagrams



Three-State High Load Circuit



THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

© Copyright Intersil Americas LLC 1999. All Rights Reserved.

All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

Die Characteristics

DIE DIMENSIONS:
 106mils x 108mils
 2.68mm x 2.74mm

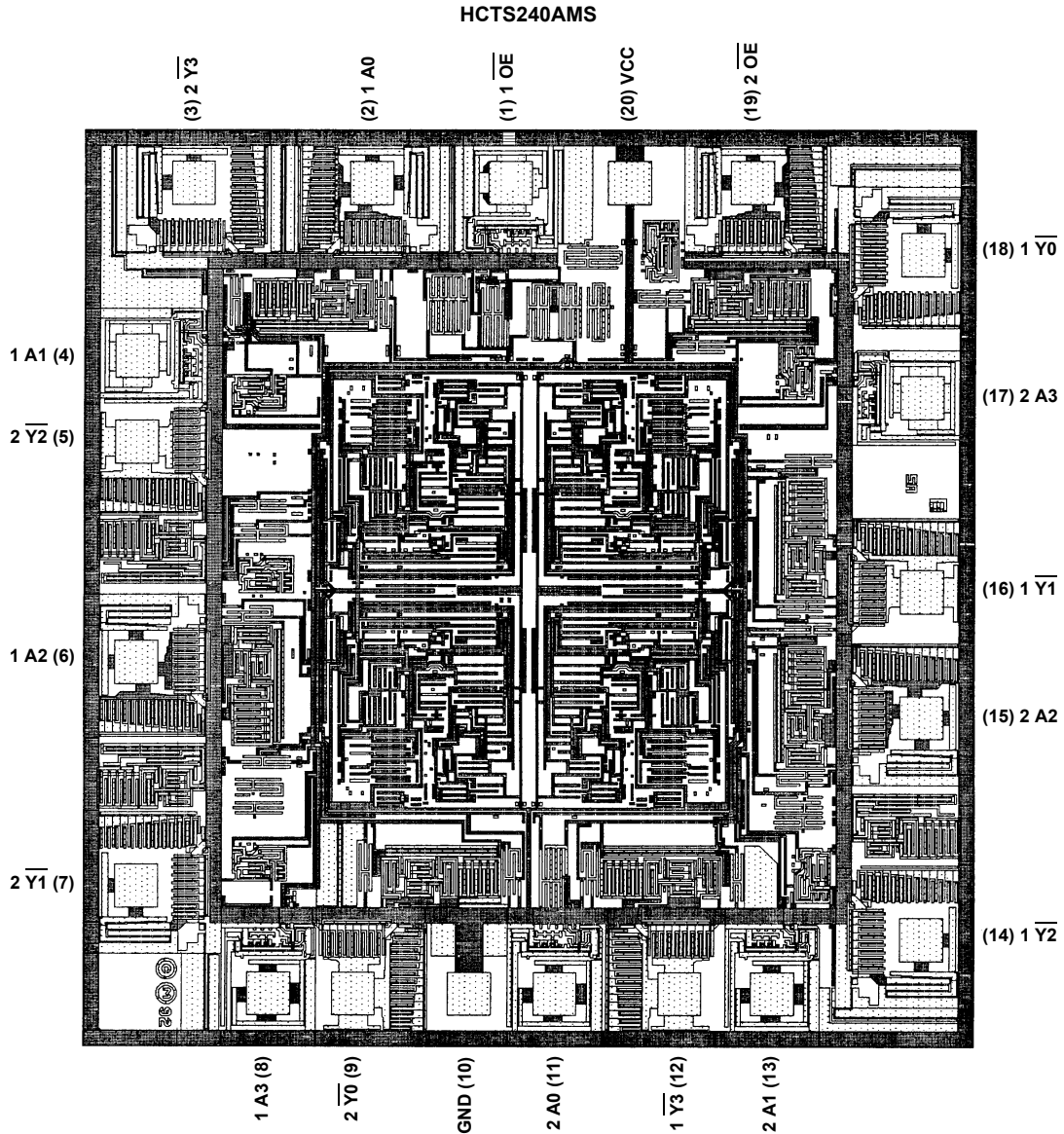
METALLIZATION:
 Type: SiAl
 Metal Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:
 Type: SiO_2
 Thickness: $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:
 $<2.0 \times 10^5 \text{A/cm}^2$

BOND PAD SIZE:
 $100\mu\text{m} \times 100\mu\text{m}$
 4 mils x 4 mils

Metallization Mask Layout



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS240A is TA14400B.