SPEED/PACKAGE AVAILABILITY

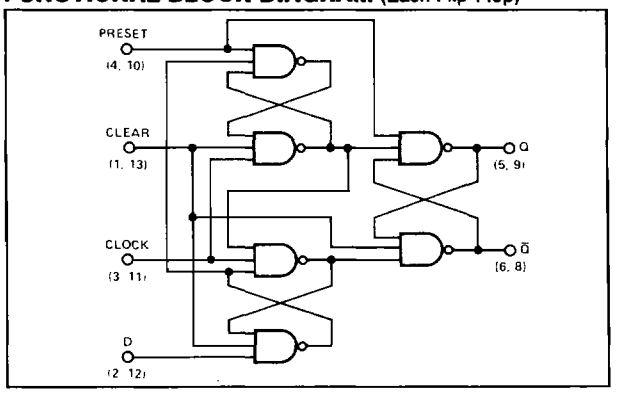
54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

DESCRIPTION

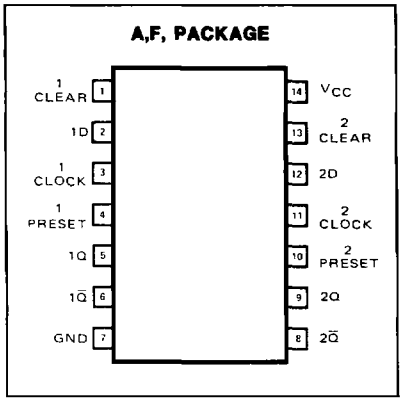
These monolithic dual edge-triggered D-type flip-flops feature individual D, clock, preset, and clear inputs.

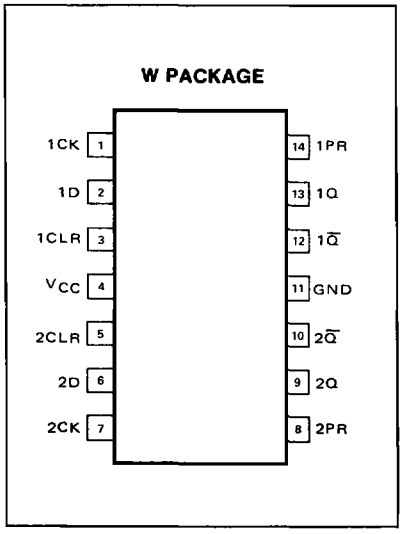
Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



PIN CONFIGURATION





TRUTH TABLE (Each Flip-Flop)

	Inputs			Outputs	
Preset	Clear	Clock	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state) L = low level (steady state)
*This condition is nonstable. It will not remain after clear and preset return to their inactive (high) state.

LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	25		35	43		25	33		75	90		MHz
$t_{w(Clock)}$	Width of clock input pulse									25						
	Clock high			30			15						6			ns
	Clock low			37			13.5						7.3			
$t_{w(Clear}$	Width of clear input pulse			30			25			25			7			ns
$t_{w(Preset)}$	Width of preset input pulse			30			25			25			7			ns
t_{Setup}	Input setup time			20↑	15								3↓			ns
	High level						10↑			25						
	Low level						15↑			20						
t_{Hold}	Input hold time			5↑	2		5↑			5			2↓			ns
Propagation delay time																
t_{PLH}	Low-to-high	Clear, Preset				25			20		8	25		5	6	ns
															CLK=1	
														8	13.5	
															CLK=0	
t_{PHL}	High-to-low					40			30		16	40		5	8	
t_{PHL}	Low-to-high	Clock		10	14	25	4	8.5	15		8	25		7	9	ns
t_{PHL}	High-to-low			10	20	40		13	20		16	40		7	9	

Load circuit and typical waveforms are shown at the front of section.

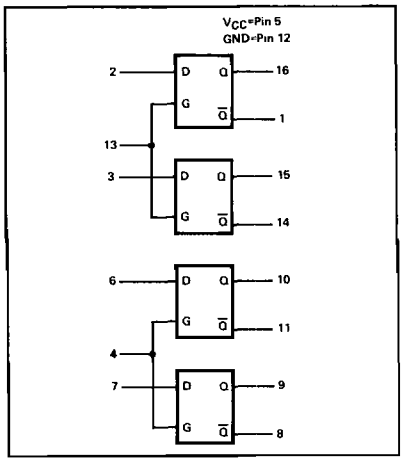
SPEED/PACKAGE AVAILABILITY

54	F	74	B,F
54LS	F,W	74LS	B,F

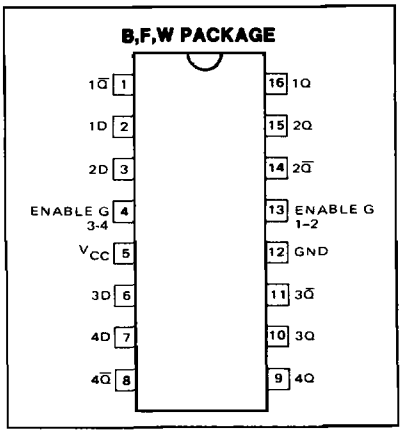
DESCRIPTION

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_w Width of enabling pulse						20			
t_{Setup} Input setup time						20			
High level				7	20				
Low level				14	20				
t_{Hold} Input hold time						0			
High Level			0	15					
Low level			0	6					
Propagation delay time									
t_{PLH} Low-to-high	D	Q		16	30		15	27	ns
t_{PHL} High-to-low				14	25		9	17	
t_{PLH} Low-to-high	D	$\overline{Q}$		24	40		12	20	ns
t_{PHL} High-to-low				7	15		7	15	
t_{PHL} Low-to-high	G	Q		16	30		15	27	ns
t_{PHL} High-to-low				7	15		14	25	
t_{PLH} Low-to-high	G	$\overline{Q}$		16	30		16	30	ns
t_{PHL} High-to-low				7	15		7	15	

Load circuit and typical waveforms are shown at the front of section

TRUTH TABLE (Each Latch)

LOGIC 54/74

(Each Latch)		
t_n	t_n+1	
D	Q	$\overline{Q}$
1	1	0
0	0	1

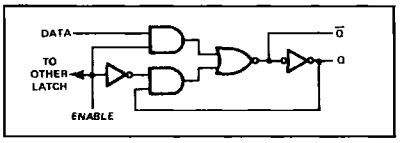
NOTES:
1. t_n = bit time before clock pulse
2. t_n+1 = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

54/74LS

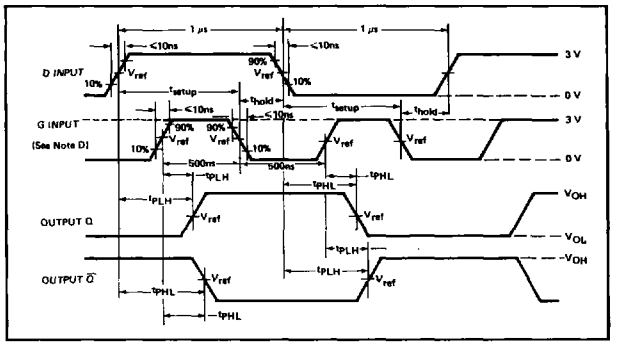
INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level,
X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

FLIP-FLOP LOGIC DIAGRAM

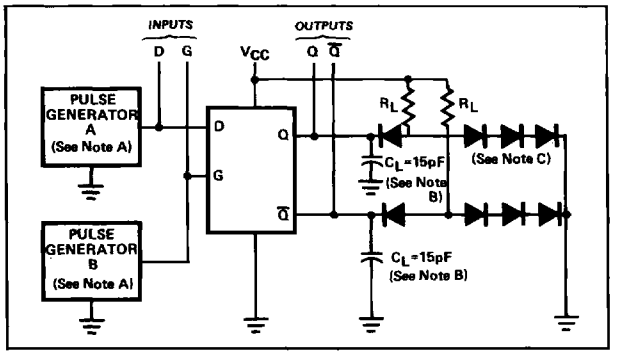


PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. The pulse generators have the following characteristics: Z_{out} ≈ 50 Ω; for pulse generator A, PRR ≤ 500 kHz; for pulse generator B, PRR ≤ 1 MHz. Positions of D and G input pulses are varied with respect to each other to verify setup times.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. When measuring propagation delay times from the D input, the corresponding G input must be held high.
E. V_{ref} = 1.3V.



TEST CIRCUIT

LOGIC