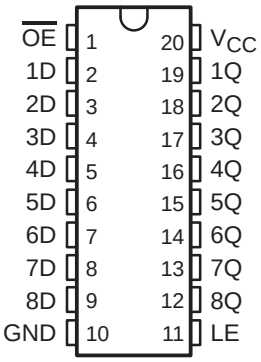
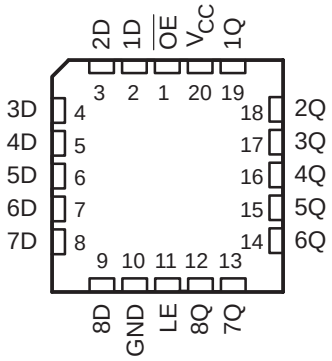
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **True Logic Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages**

**SN54ALS573C, SN54AS573A . . . J OR W PACKAGE**
**SN74ALS573C, SN74AS573A . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54ALS573C, SN54AS573A . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, outputs (Q) respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

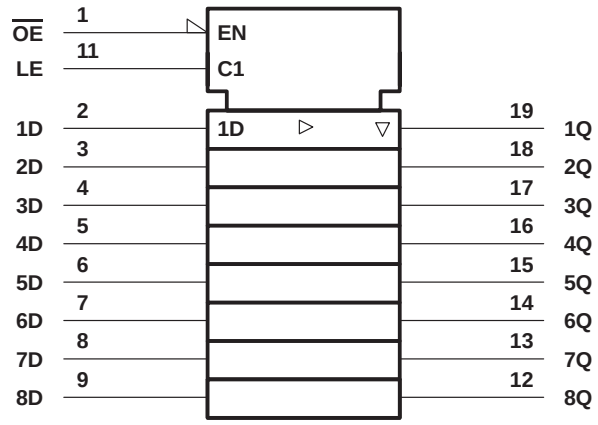
$\overline{OE}$ does not affect internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS573C and SN54AS573A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS573C and SN74AS573A are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each latch)**

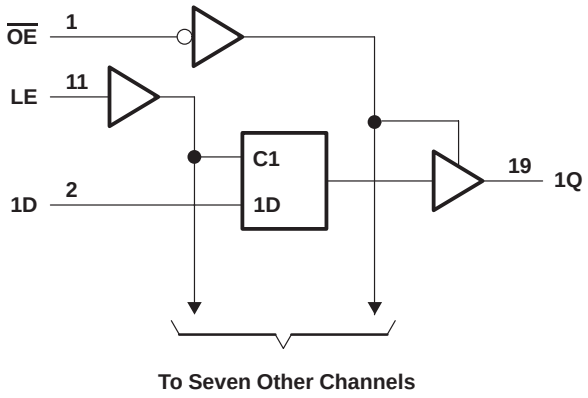
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

### logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, $T_A$: SN54ALS573C . . . . . –55°C to 125°C
SN74ALS573C . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | SN54ALS573C | | | SN74ALS573C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | –1 | | | –2.6 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | | | 24 | mA |
| $t_w$ | Pulse duration, LE high | 25 | | | 10 | | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 10 | | | 10 | | | ns |
| $t_h$ | Hold time, data after LE↓ | 7 | | | 7 | | | ns |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54ALS573C | | | SN74ALS573C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$ –2 | | | $V_{CC}$ –2 | | | V |
| | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | 2.4 | 3.3 | | | | | |
| | | $I_{OH}$ = –2.6 mA | | | | 2.4 | 3.2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | –20 | | | –20 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.13 | | | –0.1 | mA |
| $I_O$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –20 | | –112 | –30 | | –112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 10 | 17 | | 10 | 17 | mA |
| | | Outputs low | | 15 | 24 | | 15 | 24 | |
| | | Outputs disabled | | 16 | 27 | | 16 | 27 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS573C | | SN74ALS573C | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | 2 | 20 | 2 | 14 | ns |
| $t_{PHL}$ | | | 2 | 17 | 2 | 14 | |
| $t_{PLH}$ | LE | Q | 8 | 33 | 6 | 20 | ns |
| $t_{PHL}$ | | | 8 | 24 | 6 | 19 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 4 | 28 | 3 | 18 | ns |
| $t_{PZL}$ | | | 4 | 21 | 4 | 18 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 2 | 20 | 1 | 10 | ns |
| $t_{PLZ}$ | | | 3 | 26 | 1 | 15 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, $T_A$: SN54AS573A . . . . . –55°C to 125°C
SN74AS573A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | SN54AS573A | | | SN74AS573A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | –12 | | | –15 | mA |
| $I_{OL}$ | Low-level output current | | | 32 | | | 48 | mA |
| $t_w$* | Pulse duration, LE high | 5.5 | | | 4.5 | | | ns |
| $t_{su}$* | Setup time, data before LE↓ | 2 | | | 2 | | | ns |
| $t_h$* | Hold time, data after LE↓ | 3 | | | 3 | | | ns |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54AS573A | | | SN74AS573A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –2 mA | $V_{CC}$ –2 | | | $V_{CC}$ –2 | | | V |
| | $V_{CC}$ = 4.5 V | $I_{OH}$ = –12 mA | 2.4 | 3.2 | | | | | |
| | | $I_{OH}$ = –15 mA | | | | 2.4 | 3.3 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 32 mA | | 0.28 | 0.5 | | | | V |
| | | $I_{OL}$ = 48 mA | | | | | 0.33 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | –50 | | | –50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.1 | | | –0.5 | mA |
| $I_O$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | –30 | | –112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 56 | 93 | | 56 | 93 | mA |
| | | Outputs low | | 55 | 90 | | 55 | 90 | |
| | | Outputs disabled | | 65 | 106 | | 65 | 106 | |

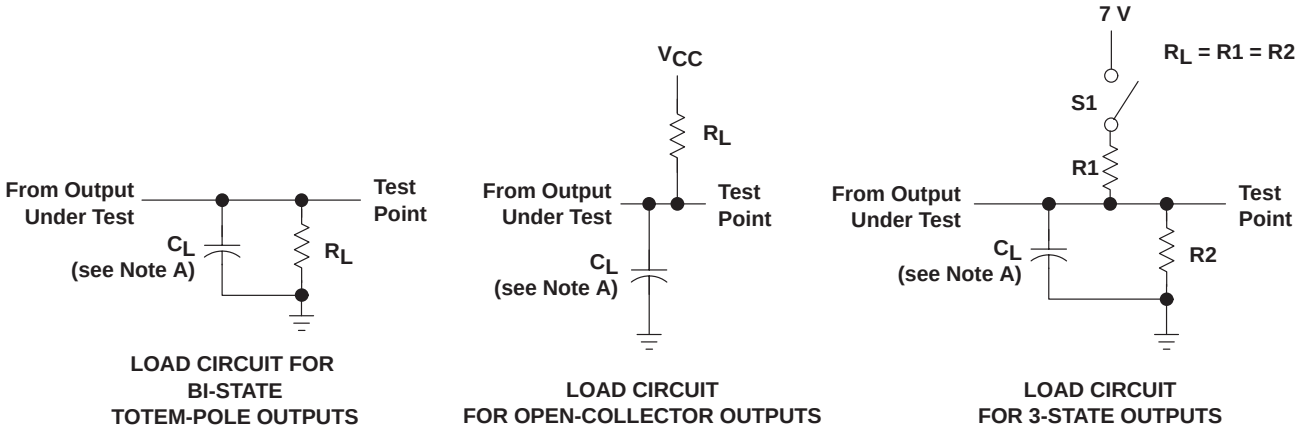
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS573A | | SN74AS573A | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | 3 | 11 | 3 | 8 | ns |
| $t_{PHL}$ | | | 3 | 8 | 3 | 7 | |
| $t_{PLH}$ | LE | Q | 6 | 16.5 | 6 | 13 | ns |
| $t_{PHL}$ | | | 4 | 9 | 4 | 7.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 2 | 8 | 2 | 6.5 | ns |
| $t_{PZL}$ | | | 4 | 11 | 4 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 2 | 8 | 2 | 6.5 | ns |
| $t_{PLZ}$ | | | 2 | 8 | 2 | 7 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

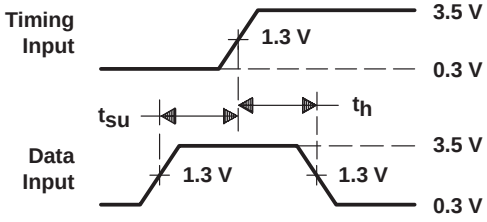
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



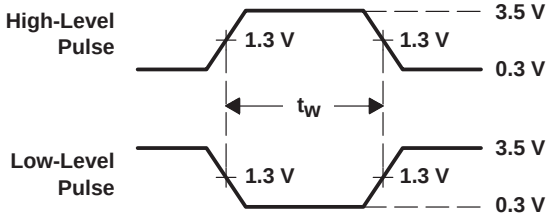

LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

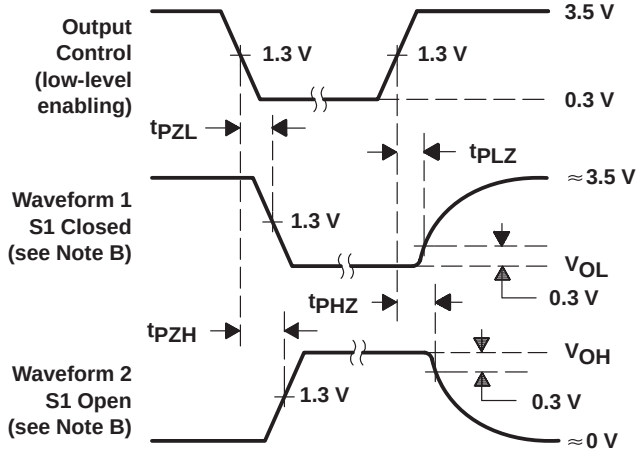
LOAD CIRCUIT FOR 3-STATE OUTPUTS



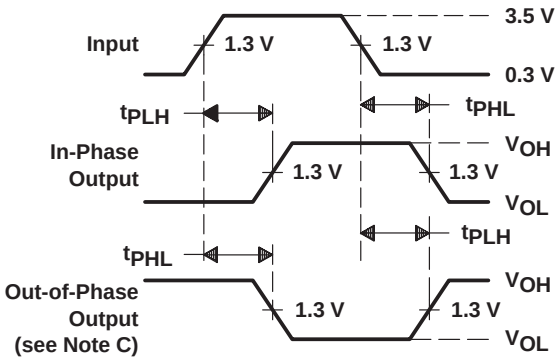

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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# SN74ALS573C, Octal D-Type Transparent Latches With 3-State Outputs

DEVICE STATUS: **ACTIVE**

| PARAMETER NAME | SN54ALS573C | SN74ALS573C |
|---|---|---|
| Voltage Nodes (V) | 5 | 5 |
| Vcc range (V) | 4.5 to 5.5 | 4.5 to 5.5 |
| Input Level | TTL | TTL |
| Output Level | TTL | TTL |
| Output Drive (mA) | | -2.6/24 |
| No. of Outputs | 8 | 8 |
| Static Current | | 20.5 |
| th (ns) | | 7 |
| tpd max (ns) | | 14 |
| tsu (ns) | | 10 |
| Logic | True | True |

## FEATURES

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- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- True Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

## DESCRIPTION

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These octal D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, outputs (Q) respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS573C and SN54AS573A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS573C and SN74AS573A are characterized for operation from 0°C to 70°C.

## TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

## DATASHEET

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Full datasheet in Acrobat PDF: sn74als573c.pdf (109 KB,Rev.D) (Updated: 01/01/1995)

## APPLICATION NOTES

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View Application Notes for Digital Logic

- Advanced Schottky (ALS and AS) Logic Families (SDAA010 - Updated: 08/01/1995)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

## RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

## PRICING/AVAILABILITY/PKG

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| DEVICE INFORMATION | | | | | | | TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002 | | | REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ORDERABLE DEVICE | STATUS | PACKAGE TYPE\|PINS | TEMP (°C) | PRODUCT CONTENT | BUDGETARY PRICING QTY \| $US | STD PACK QTY | IN STOCK | IN PROGRESS QTY\|DATE | LEAD TIME | DISTRIBUTOR COMPANY\|REGION | IN STOCK | PURCHASE |
| SN74ALS573CDBLE | OBSOLETE | SSOP (DB) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74ALS573CDBR | ACTIVE | SSOP (DB) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.55 | 2000 | N/A* | 4000 \| 03 Oct | 5 WKS | | | |
| SN74ALS573CDW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.55 | 25 | 1938 | 637 \| 30 Sep | 5 WKS | Avnet \| AMERICA | >1k | BUY NOW |
| | | | | | | | | 1000 \| 03 Oct | | DigiKey \| AMERICA | 481 | BUY NOW |
| SN74ALS573CDWR | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.57 | 2000 | 4000 | >10k \| 15 Oct | 5 WKS | Avnet \| AMERICA | >1k | BUY NOW |
| | | | | | | | | | | DigiKey \| AMERICA | >1k | BUY NOW |
| SN74ALS573CN | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.55 | 20 | 20 | 77 \| 25 Sep | 5 WKS | Avnet \| AMERICA | >1k | BUY NOW |
| | | | | | | | | 2020 \| 03 Oct | | DigiKey \| AMERICA | >1k | BUY NOW |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALS573CN3 | OBSOLETE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74ALS573CNSR | ACTIVE | SOP (NS) \| 20 | | View Contents | 1KU \| 0.55 | 2000 | N/A* | 1797 \| 23 Sep | 5 WKS | | | |
| | | | | | | | | 1467 \| 26 Sep | | | | |
| | | | | | | | | 736 \| 02 Oct | | | | |
| | | | | | | | | 4000 \| 14 Oct | | | | |

**Table Data Updated on: 9/26/2002**