



MM54HC640/MM74HC640 Inverting Octal TRI-STATE® Transceiver

MM54HC643/MM74HC643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional buffers utilize advanced silicon-gate CMOS technology, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

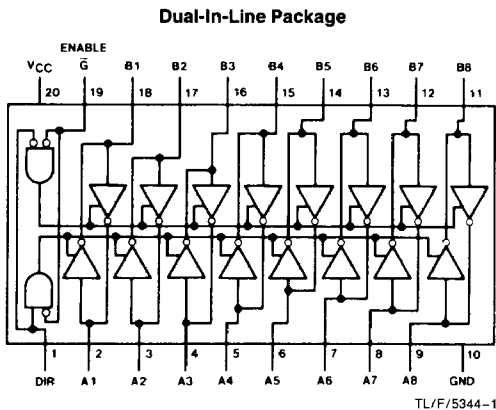
Each device has an active low enable \bar{G} and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC640/MM74HC640 transfers inverted data from one bus to other and the MM54HC643/MM74HC643 transfers inverted data from the A bus to the B bus and true data from the B bus to the A bus.

These devices can drive up to 15 LS-TTL Loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

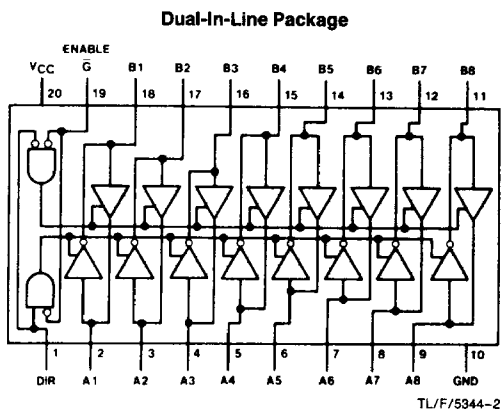
- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μ A maximum (74 HC)
- TRI-STATE outputs for connection to bus oriented systems
- High output drive: 6 mA (min)

Connection Diagrams



Order Number MM54HC640* or MM74HC640*

*Please look into Section 8, Appendix D for availability of various package types.



Order Number MM54HC643* or MM74HC643*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Control Inputs		Operation	
\bar{G}	DIR	640	643
L	L	\bar{B} data to A bus	B data to A bus
L	H	\bar{A} data to B bus	\bar{A} data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage DIR and \bar{G} pins (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{IN} , V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{CD})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN} , V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise/Fall Times (t_r , t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			Units	
				74HC $T_A = -40$ to $85^\circ C$	54HC $T_A = -55$ to $125^\circ C$			
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V	
			4.5V	3.15	3.15	3.15	V	
			6.0V	4.2	4.2	4.2	V	
V_{IL}	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V	
			4.5V	1.35	1.35	1.35	V	
			6.0V	1.8	1.8	1.8	V	
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current (\bar{G} and DIR)	$V_{IN} = V_{CC}$ or GND	6.0V	± 0.1	± 1.0	± 1.0	μA	
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Enable $\bar{G} = V_{IH}$	6.0V	± 0.5	± 5.0	± 10	μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V	8.0	80	160	μA	

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C, t_r = t_f = 6 ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 45 pF$	13	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$ $C_L = 45 pF$	33	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 5 pF$	32	42	ns

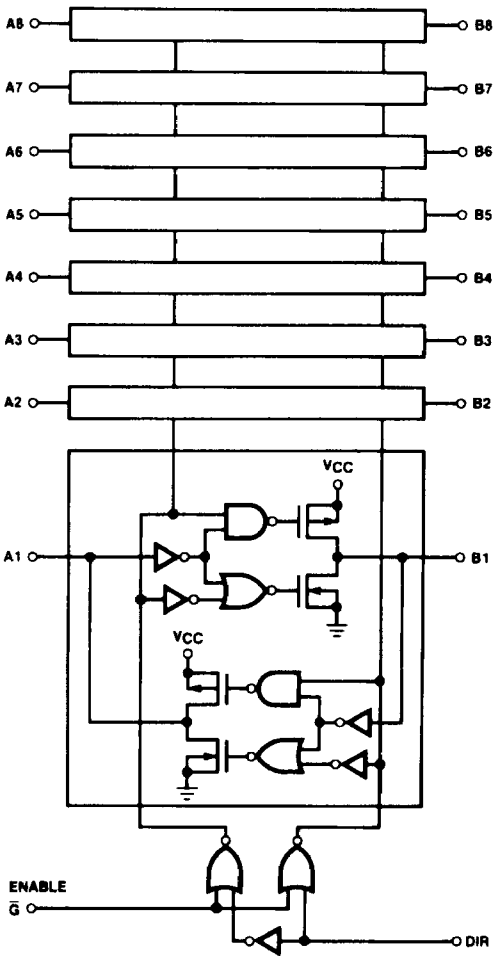
AC Electrical Characteristics $V_{CC} = 2.0V to 6.0V, C_L = 50 pF, t_r = t_f = 6 ns$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74HC		54HC		Units							
						$T_A = -40 to 85^\circ C$		$T_A = -55 to 125^\circ C$									
				Typ							Guaranteed Limits						
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 50 pF$	2.0V	29	72	88		96		ns							
			2.0V	38	96	116		128		ns							
		$C_L = 150 pF$	4.5V	14	18	22		24		ns							
			4.5V	18	24	29		32		ns							
		$C_L = 50 pF$	6.0V	14	18	22		24		ns							
			6.0V	18	24	29		32		ns							
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L = 1 k\Omega$	$C_L = 50 pF$	2.0V	70	184	224		240		ns						
				2.0V	80	216	260		284		ns						
		$C_L = 150 pF$	4.5V	35	46	56		60		ns							
			4.5V	41	54	65		71		ns							
		$C_L = 50 pF$	6.0V	31	41	50		54		ns							
			6.0V	36	47	57		62		ns							
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 50 pF$	2.0V	47	172	208		224		ns							
			4.5V	33	43	52		56		ns							
			6.0V	31	41	50		54		ns							
t_{THL}, t_{TLH}	Output Rise and Fall Time	$C_L = 50 pF$	2.0V	20	60	75		90		ns							
			4.5V	6	12	15		18		ns							
			6.0V	5	10	13		15		ns							
C_{PD}	Power Dissipation Capacitance (Note 5)	$\bar{G} = V_{IL}$ $\bar{G} = V_{IH}$		120					pF								
C_{IN}	Maximum Input Capacitance			5	10	10		10		pF							
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20		20		pF							

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

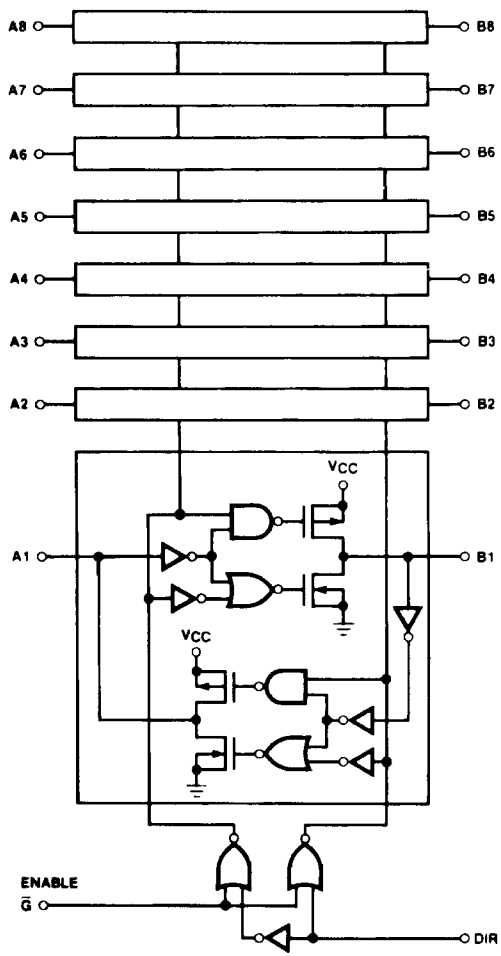
Logic Diagrams

'HC640



TL/F/5344-5

'HC643



TL/F/5344-6