



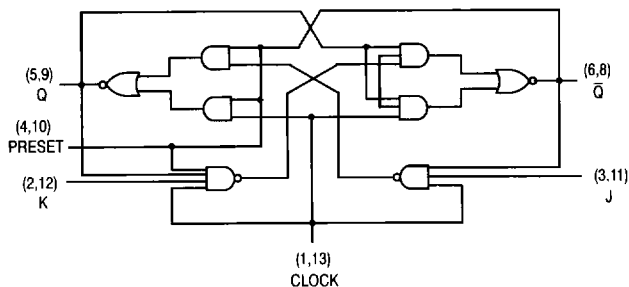
MOTOROLA

Dual J-K Flip-Flop With Preset

**ELECTRICALLY TESTED PER:
MIL-M-38510/30104**

The 54LS113A offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT — TRUTH TABLE						
Operating Mode	Inputs			Outputs		
	PR	J	K	Q	Q̄	
Set	L	X	X	H	L	
Toggle	H	h	h	q̄	q	
Load "0" (Reset)	H	l	h	L	H	
Load "1" (Set)	H	h	l	H	L	
Hold	H	l	l	q	q̄	

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

X = Don't Care

l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

Military 54LS113A



AVAILABLE AS:

- 1) JAN: JM38510/30104BXA
- 2) SMD: N/A
- 3) 883: 54LS113A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

PIN ASSIGNMENTS

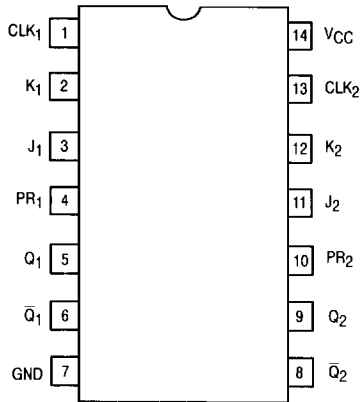
FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
CLK ₁	1	1	2	VCC
K ₁	2	2	3	VCC
J ₁	3	3	4	VCC
PR ₁	4	4	6	GND
Q ₁	5	5	8	VCC
Q̄ ₁	6	6	9	OPEN
GND	7	7	10	GND
Q̄ ₂	8	8	12	OPEN
Q ₂	9	9	13	VCC
PR ₂	10	10	14	GND
J ₂	11	11	16	VCC
K ₂	12	12	18	VCC
CLK ₂	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:

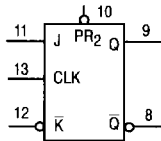
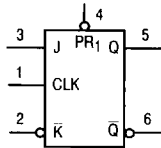
VCC = 5.0 V MIN/6.0 V MAX

54LS113A

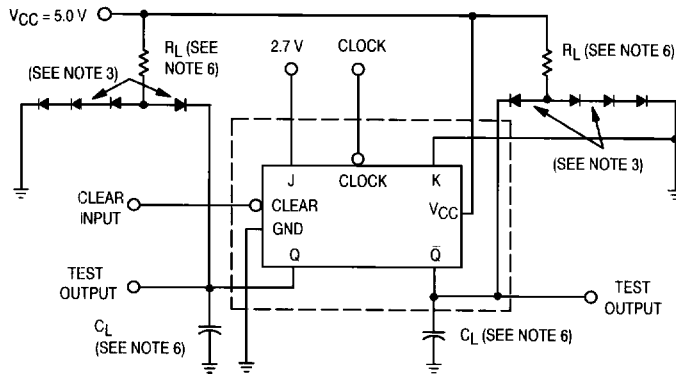
CONNECTION DIAGRAM



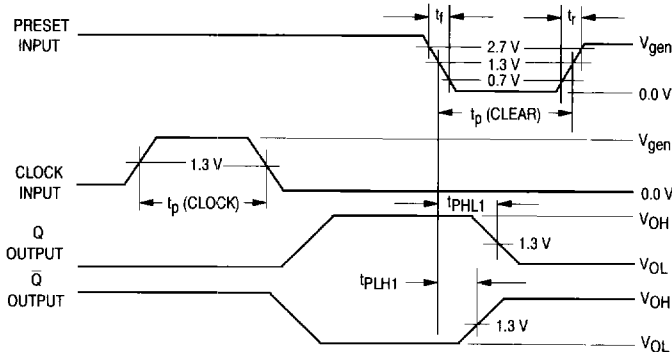
LOGIC SYMBOL



CLEAR SWITCHING TEST CIRCUIT



WAVEFORMS

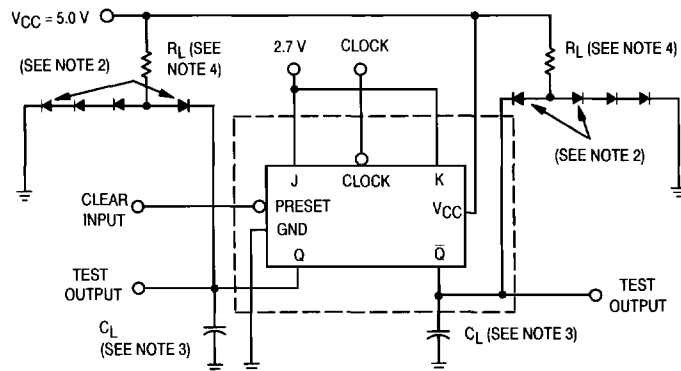


NOTES:

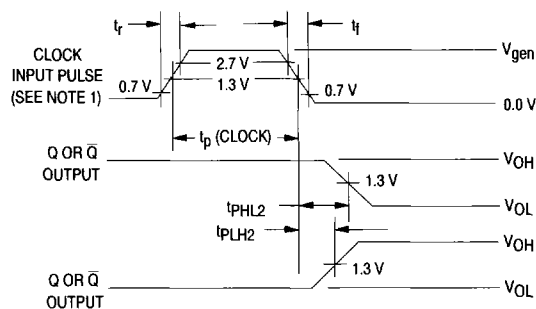
1. Preset inputs dominate regardless of the state of the clock or J-K inputs.
2. Preset input pulse characteristics:
 $V_{gen} = 3.0\text{ V}$, $t_r \leq 15\text{ ns}$, $t_f \leq 6.0\text{ ns}$,
 $t_p(\text{preset}) = 30\text{ ns}$, $\text{PRR} \leq 1.0\text{ MHz}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. Voltage measurements are to be made with respect to network ground terminal.
6. $R_L = 2.0\text{ k}\Omega \pm 5.0\%$.
7. Clock input pulse characteristics:
 $V_{gen} = 3.0\text{ V}$, $t_p(\text{clock}) \leq 25\text{ ns}$,
 $\text{PRR} \leq 1.0\text{ MHz}$.

54LS113A

SYNCHRONOUS SWITCHING TEST CIRCUIT



WAVEFORMS





NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output):
 $V_{gen} = 3.0\text{ V}$, $t_r \leq 15\text{ ns}$, $t_f = 6.0\text{ ns}$, $t_p\text{ (clock)} = 20\text{ ns}$ and $PRR \leq 1.0\text{ MHz}$. When testing f_{MAX} the clock input characteristics are: $V_{gen} = 3.0\text{ V}$, $t_r = t_f \leq 6.0\text{ ns}$, $t_p\text{ (clock)} \leq 20\text{ ns}$ and $PRR =$ (see table).
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2.0\text{ k}\Omega \pm 5.0\%$.

54LS113A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)	
	Static Parameters:	+ 25°C		+ 125°C		– 55°C				
		Subgroup 1		Subgroup 2		Subgroup 3				
		Min	Max	Min	Max	Min	Max			
V _{OH}	Logical “1” Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = – 0.4 mA, V _{IN} = 2.0 V, V _{IL} = 0.7 V.	
V _{OL}	Logical “0” Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IH} = 2.0 V, V _{IL} = 0.7 V.	
V _{IC}	Input Clamping Voltage		– 1.5					V	V _{CC} = 4.5 V, I _{IN} = – 18 mA, other inputs are open.	
I _{IH}	Logical “1” Input Current (J & K inputs)		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other input = GND.	
I _{IHH}	Logical “1” Input Current (J & K inputs)		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, PR = 4.5 V, K = GND, CLK = (see note 1).	
I _{IH}	Logical “1” Input Current (PR inputs)		60		60		60	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, J = 4.5 V, CLK & K = GND, Q = (see note 3).	
I _{IHH}	Logical “1” Input Current (PR inputs)		300		300		300	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, J = 4.5 V, CLK & K = GND, Q = (see note 3).	
I _{IH}	Logical “1” Input Current (CLK inputs)		80		80		80	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs = GND.	
I _{IHH}	Logical “1” Input Current (CLK inputs)		400		400		400	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs = GND.	
I _{IL}	Logical “0” Input Current (J & K inputs)	– 0.12	– 0.36	– 0.12	– 0.36	– 0.12	– 0.36	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, CLK = 4.5 V, J = 0 V, PR = (see note 2).	
I _{IL}	Logical “0” Input Current (CLK inputs)	– 0.24	– 0.72	– 0.24	– 0.72	– 0.24	– 0.72	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, J & K = 4.5 V, PR = (see note 2).	
I _{IL}	Logical “0” Input Current (PR inputs)	– 0.12	– 0.72	– 0.12	– 0.72	– 0.12	– 0.72	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, other inputs = 4.5 V.	
I _{OS}	Output Short Circuit Current	Q ₁ & Q ₂	– 15	– 100	– 15	– 100	– 15	– 100	mA	V _{CC} = 5.5 V, Q = GND. PR = GND, other inputs are open. J = GND, V _{IN} = 4.5 V, CLK = (see note 1), V _{OUT} = 2.25 V.
		\bar{Q}_1 & \bar{Q}_2	– 7.5	– 50	– 7.5	– 50	– 7.5	– 50		
I _{CC}	Power Supply Current		8.0		8.0		8.0	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, CLK = (see note 1), J = GND.	
									V _{CC} = 5.5 V, PR = GND, other inputs are 5.5 V.	
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.	
V _{IL}	Logical “0” Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.	
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 4.5 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.	

NOTES: 1. =  0.0 V 2.5 V min/5.5 V max 2. =  0.0 V 2.5 V min/5.5 V max 3. Momentary GND, then open.

54LS113A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0 —	28 20	5.0 —	40 35	5.0 —	40 35	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0 —	21 20	5.0 —	32 27	5.0 —	32 27	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0 —	30 20	5.0 —	42 37	5.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH2} t _{PLH2}	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0 —	22 20	5.0 —	32 27	5.0 —	32 27	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
f _{MAX}	Maximum Clock Frequency	25		25		25		MHz	V _{CC} = 5.0 V, V _{IN} = 2.7 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%.
f _{MAX}	Maximum Clock Frequency	30						MHz	V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.

NOTES:

1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.