HADC674Z

FAST, COMPLETE 12-BIT µP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

FEATURES:

- **IMPROVED PIN-TO-PIN COMPATIBLE MONOLITHIC VERSION OF THE HI574A AND AD674A**
- **Complete 12-bit A/D Converter with Sample-Hold, Reference and Clock**
- **Low Power Dissipation (150mW Max)**
- 12-bit Linearity (over temp)
- 15µs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS:

- **MILITARY/INDUSTRIAL DATA ACQUISITION SYSTEMS**

- 8 OR 12-bit µP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

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GENERAL DESCRIPTION

The HADC674Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI674A and AD674A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The HADC674Z features 15µs (Max) conversion time of 10 or 20 Volt input signals. Also, a 3-state output buffer is added for direct interface to an 8-, 12-, or 16-bit µP bus.

The HADC674Z is manufactured on Honeywell SPT's Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC674Z has standard bipolar and unipolar input ranges of 10V and 20V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM
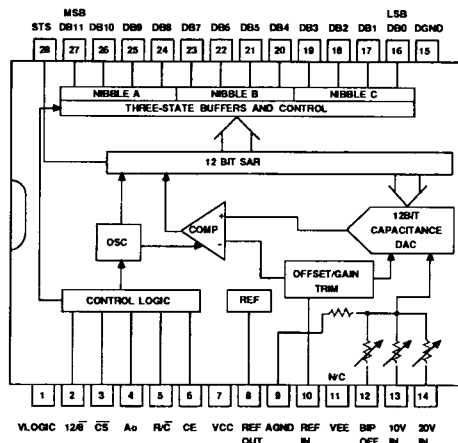
ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
Positive Supply Voltage (V_{CC} to DGND)...0 to +16.5V
Logic Supply Voltage (V_{LOGIC} to DGND)...........0 to +7V
Analog to Digital Ground (AGND to DGND)...-0.5 to +1V

Input Voltages
Control Input Voltages (to DGND).
(CE, $\overline{CS}$, Ao, 12/8, R/$\overline{C}$)...................-0.5 to V_{LOGIC} +0.5V
Analog Input Voltage (to AGND)...........................±16.5V
(REF IN, BIP OFF, 10Vin)
20V Vin Input Voltage (to AGND)...........................±24V

Output
Reference Output Voltage.........Indefinite short to GND
Momentary short to V_{CC}

Temperature
Operating Temperature, ambient.-55 to +125(case) °C
junction....................+175 °C
Lead Temperature, (soldering 10 seconds).......+300 °C
Storage Temperature................................-65 to +150 °C
Power Dissipation..1000mW
Thermal Resistance (θ_{jA})..................................48°C/W

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

COMMERCIAL TEMPERATURE RANGE: 0 TO +70°C

T_A = 0 to 70°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCC MIN TYP MAX	HADC674ZBC MIN TYP MAX	HADC674ZAC MIN TYP MAX	UNITS

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LEVEL	CC MIN	CC TYP	CC MAX	BC MIN	BC TYP	BC MAX	AC MIN	AC TYP	AC MAX	UNITS
Resolution				12			12			12		BITS
Linearity Error		I		±1			$\pm\frac{1}{2}$			$\pm\frac{1}{2}$		LSB
Differential Linearity Error		I		±1			$\pm\frac{1}{2}$			$\pm\frac{1}{2}$		LSB
Unipolar Offset ; 10V, 20V	+25°C Adjustable to zero	I		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset[1]; ±5V, ±10V	+25°C Adjustable to zero	I		±10			±4			±4		LSB
Full Scale Calibration Error[1] All Ranges	+25°C Adjustable to zero	I		0.3			0.3			0.3		% of FS
	No adjustment at +25°C	II		0.5			0.4			0.35		% of FS
	With adjustment at +25°C	II		0.22			0.12			0.05		% of FS
Temperature Coefficients	Using internal reference											
Unipolar Offset		I		±0.2	±2 (10)		±0.1	±1 (5)		±0.1	±1 (5)	LSB (ppm/°C)
Bipolar Offset		I		±0.2	±2 (10)		±0.1	±1 (5)		±0.1	±1 (5)	LSB (ppm/°C)
Full Scale Calibration		I		±9 (45)			±5 (25)			±2 (10)		LSB (ppm/°C)

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

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COMMERCIAL TEMPERATURE RANGE: 0 TO +70°C

T_A = 0 to 70°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

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PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCC MIN TYP MAX	HADC674ZBC MIN TYP MAX	HADC674ZAC MIN TYP MAX	UNITS

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LEVEL	CC MIN	CC TYP	CC MAX	BC MIN	BC TYP	BC MAX	AC MIN	AC TYP	AC MAX	UNITS
Power Supply Rejection	Max change in full scale calibration											
+13.5V<Vcc<+16.5V or +11.4V<Vcc<+12.6V		I		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5V<V_{LOGIC}<+5.5V		I		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Inputs Ranges		I	-5		+5	-5		+5	-5		+5	VOLTS
Bipolar			-10		+10	-10		+10	-10		+10	VOLTS
Unipolar		I	0		+10	0		+10	0		+10	VOLTS
			0		+20	0		+20	0		+20	VOLTS
Input Impedance 10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	VOLTS
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	VOLTS
V_{EE}	Not required for circuit operation.											
Operating Current I_{LOGIC}		I		0.5	1		0.5	1		0.5	1	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation +15V, +5V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current[2]		I			2			2			2	mA

Note 2: Available for external loads, external load should not change during conversion.
When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output.

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COMMERCIAL TEMPERATURE RANGE: 0 TO +70°C

T_A = 0 to 70°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCC MIN TYP MAX	HADC674ZBC MIN TYP MAX	HADC674ZAC MIN TYP MAX	UNITS
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0,12/$\overline{8}$)						
Logic "1"		I	2.0 5.5	2.0 5.5	2.0 5.5	VOLTS
Logic "0"		I	-0.5 +0.8	-0.5 +0.8	-0.5 +0.8	VOLTS
Current	0 to 5.5V Input	I	±.01 +5	±.01 +5	±.01 +5	µA
Capacitance		II	5	5	5	pF
Logic Outputs (DB11-DB0, STS)						
Logic "0"	(I_{Sink} = 1.6mA)	I	+0.4	+0.4	+0.4	VOLTS
Logic "1"	(I_{SOURCE} = 500µA)	I	+2.4	+2.4	+2.4	VOLTS
Leakage	(High Z State, DB11- DB0 Only)	I	-5 ±0.1 +5	-5 ±0.1 +5	-5 ±0.1 +5	µA
Capacitance		II	5	5	5	pF

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INDUSTRIAL TEMPERATURE RANGE -25 TO +85°C

T_A = -25 to 85°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCI MIN TYP MAX	HADC674ZBI MIN TYP MAX	HADC674ZAI MIN TYP MAX	UNITS

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LEVEL	CI MIN	CI TYP	CI MAX	BI MIN	BI TYP	BI MAX	AI MIN	AI TYP	AI MAX	UNITS
Resolution					12			12			12	BITS
Linearity Error	25°C	I			±1			±$\frac{1}{2}$			±$\frac{1}{2}$	LSB
Linearity Error		I			±1			±$\frac{1}{2}$			±$\frac{1}{2}$	LSB
Differential Linearity Error		I			±1			±$\frac{1}{2}$			±$\frac{1}{2}$	LSB
Unipolar Offset; 10V, 20V	+25°C Adjustable to zero	I			±2			±2			±2	LSB
Bipolar Offset[1]; ±5V, ±10V	+25°C Adjustable to zero	I			±10			±4			±4	LSB
Full Scale Calibration Error[1] All Ranges	+25°C Adjustable to zero	I			0.3			0.3			0.3	% of FS
	No adjustment at +25°C Tmin to Tmax	II			0.7			0.5			0.4	% of FS
	With adjustment at +25°C Tmin to Tmax	II			0.4			0.2			0.1	% of FS
Temperature Coefficients	Using internal reference Tmin to Tmax											
Unipolar Offset		I			±2 (5)			±1 (2.5)			±1 (2.5)	LSB (ppm/°C)
Bipolar Offset		I			±2 (5)			±1 (2.5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration		I			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5V<Vcc<+16.5V or +11.4V<Vcc<+12.6V		I		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5V<V_{LOGIC}<+5.5V		I		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Inputs Input Ranges		I	-5		+5	-5		+5	-5		+5	VOLTS
Bipolar			-10		+10	-10		+10	-10		+10	VOLTS
		I	0		+10	0		+10	0		+10	VOLTS
Unipolar			0		+20	0		+20	0		+20	VOLTS
Input Impedance 10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

SPT

INDUSTRIAL TEMPERATURE RANGE -25 TO +85°C

T_A = -25 to 85°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCI MIN TYP MAX	HADC674ZBI MIN TYP MAX	HADC674ZAI MIN TYP MAX	UNITS

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	VOLTS
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	VOLTS
V_{EE}	Not required for circuit operation.											VOLTS
Operating Current I_{LOGIC}		I		0.5	1		0.5	1		0.5	1	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation ±15V, +5V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current[2]		I			2			2			2	mA

DIGITAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)												
Logic "1"		I	2.0		5.5	2.0		5.5	2.0		5.5	VOLTS
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	VOLTS
Current	0 to +5.5V Input	I		±.01	+5		±.01	+5		±.01	+5	µA
Capacitance		II		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6mA)	I			+0.4			+0.4			+0.4	VOLTS
Logic "1"	(I_{SOURCE} = 500µA)	I	+2.4			+2.4			+2.4			VOLTS
Leakage	(High Z State, DB11- DB0 Only)		-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		II		5			5			5		pF

Note 2   Available for external loads, external load should not change during conversion.
When supplying an external load and operating on +12V supplies, a buffer amplifier must be provided for the reference output.

SPT

MILITARY TEMPERATURE RANGE -55 TO +125°C

T_A = -55 to 125°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCM MIN TYP MAX	HADC674ZBM MIN TYP MAX	HADC674ZAM MIN TYP MAX	UNITS

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution					12			12			12	BITS
Linearity Error	25°C	I		±1			$\pm 1\frac{1}{2}$			$\pm 1\frac{1}{2}$		LSB
Linearity Error		I		±1			±1			±1		LSB
Differential Linearity Error		I		±1			$\pm 1\frac{1}{2}$			$\pm 1\frac{1}{2}$		LSB
Unipolar Offset; 10V, 20V	25°C Adjustable to zero	I		±2			±2			±2		LSB
Bipolar Offset[1]; ±5V, ±10V	25°C Adjustable to zero	I		±10			±4			±4		LSB
Full Scale Calibration Error[1] All Ranges	25°C Adjustable to zero	I		0.3			0.3			0.3		% of FS
	No adjustment at +25°C Tmin to Tmax	II		0.8			0.6			0.4		% of FS
	With adjustment at +25°C Tmin to Tmax	II		0.5			0.25			0.12		% of FS
Temperature Coefficients	Using internal reference Tmin to Tmax											
Unipolar Offset		I		±2 (5)			±1 (2.5)			±1 (2.5)		LSB (ppm/°C)
Bipolar Offset		I		±4 (10)			±2 (5)			±1 (2.5)		LSB (ppm/°C)
Full Scale Calibration		I		±20 (50)			±10 (25)			±5 (12.5)		LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5V<Vcc<+16.5V or +11.4V<Vcc<+12.6V		I		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5V<V_{LOGIC}<+5.5V		I		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Inputs Input Ranges		I	-5		+5	-5		+5	-5		+5	VOLTS
Bipolar			-10		+10	-10		+10	-10		+10	VOLTS
Unipolar		I	0		+10	0		+10	0		+10	VOLTS
			0		+20	0		+20	0		+20	VOLTS
Input Impedance 10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

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MILITARY TEMPERATURE RANGE -55 TO +125°C

T_A = -55 to 125°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCM MIN TYP MAX	HADC674ZBM MIN TYP MAX	HADC674ZAM MIN TYP MAX	UNITS

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	VOLTS
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	VOLTS
V_{EE}	Not required for circuit operation.											
Operating Current I_{LOGIC}		I		0.5	1		0.5	1		0.5	1	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation ±15V, +5V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current[2]		I			2			2			2	mA

DIGITAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)												
Logic "1"		I	2.0		5.5	2.0		5.5	2.0		5.5	VOLTS
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	VOLTS
Current	0 to +5.5V Input	I		±.01	+1		±.01	+1		±.01	+1	μA
Capacitance		II		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6mA)	I			+0.4			+0.4			+0.4	VOLTS
Logic "1"	(I_{SOURCE} = 500μA)	I	+2.4			+2.4			+2.4			VOLTS
Leakage	(High Z State, DB11-DB0 Only)		-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	μA
Capacitance		II		5			5			5		pF

Note 2 Available for external loads, external load should not change during conversion.
When supplying an external load and operating on +12V supplies, a buffer amplifier must be provided for the reference output.

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CONVERT MODE TIMING CHARACTERISTICS

Typical @ 25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC			HADC674ZB			HADC674ZA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} A0 to CE Setup		I	0			0			0			ns
t_{HAC} A0 Valid During CE High		I	50			50			50			ns
t_C Conversion Time 12-Bit Cycle	Tmin to Tmax	I	9		15	9		15	9		15	µs
8-Bit Cycle	Tmin to Tmax	I	6		10	6		10	6		10	µs

Note 5: Time is measured from 50% level of digital transitions. Tested with a 100pF and 3kΩ load for high impedance to drive and tested with 10pF and 3KΩ load for drive to high impedance.
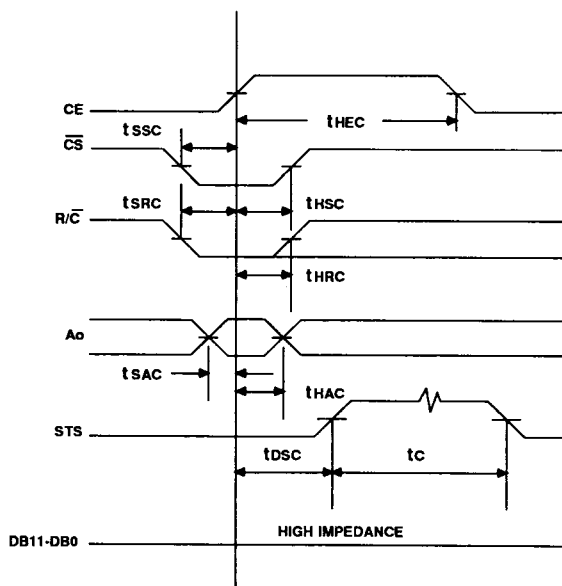
Figure 1 - Convert Mode Timing Diagram

READ MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC			HADC674ZB			HADC674ZA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST COND	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	0	0		0	0		0	0		ns
t_{HAR} A0 Valid After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns
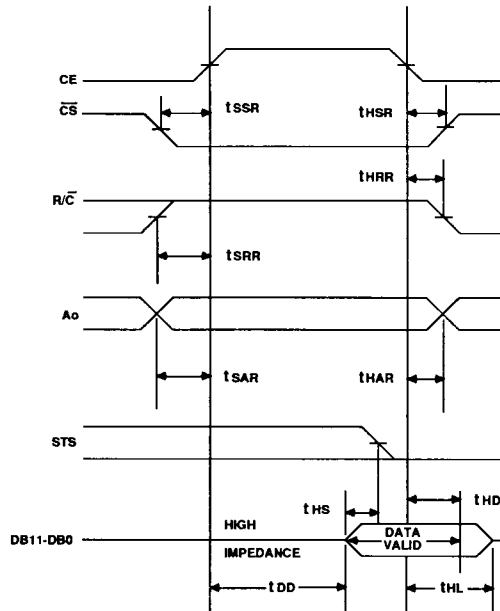
Figure 2 - Read Mode Timing Diagram

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STAND-ALONE MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER		TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC			HADC674ZB			HADC674ZA			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
AC ELECTRICAL CHARACTERISTICS													
t_{HRL}	Low R/C̄ Pulse Width		I	50			50			50			ns
t_{DS}	STS Delay from R/C̄		I			200			200			200	ns
t_{HDR}	Data Valid After R/C̄ Low		I	25			25			25			ns
t_{HS}	STS Delay After Data Valid		I	100		600	100		600	100		600	ns
t_{HRH}	High R/C̄ Pulse Width		I	150			150			150			ns
t_{DDR}	Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD													
Acquisition Time			II	1.8	2.4	3.0	1.8	2.4	3.0	1.8	2.4	3.0	µs
Aperture Uncertainty Time			II		8			8			8		ns
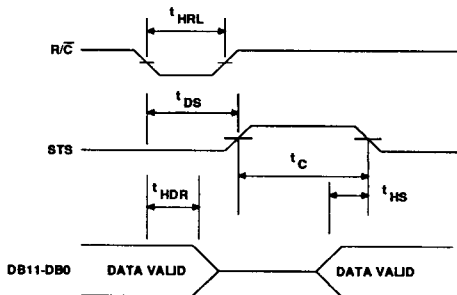
Figure 3 - Low Pulse For R/C - Outputs
Enabled After Conversion
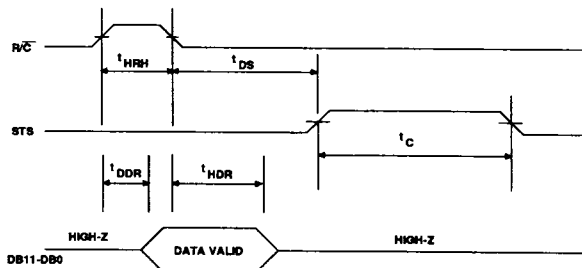
Figure 4 - High Pulse For R/C - Outputs
Enabled While R/C Is High, Otherwise
High Impedance

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_{junc} = T_{case} = T_{ambient}$.

TEST LEVEL	TEST PROCEDURE
I	Production tested at the specified conditions.
II	Parameter is guaranteed by design and sampled characterization data.

SPT

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 7). The point used as "zero" occurs 1/2LSB (1.22mV for a 10 Volt span) before the first code transistion (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC674ZAC and BC grades are guaranteed for maximum nonlinearity of ±1/2LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC674AM, BM, CC and CM grades are guaranteed to ±1LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC674Z type BC, AC, BM, and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC674Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 7 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC674Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 7 points out two missed codes in the transfer function.
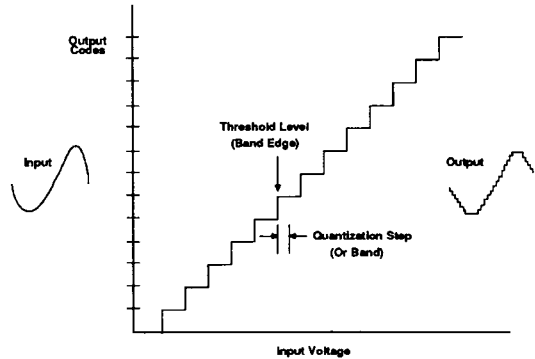
Figure 5 - Static Input Conditions

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = FSR/2^N$ where FSR = full scale range and N = 12. Non-ideal quantization bands represent differential nonlinearity errors (See Figures 5, 6 and 7).

RESOLUTION - ACTUAL VS. AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically posssible to generate 2^N unique output codes.
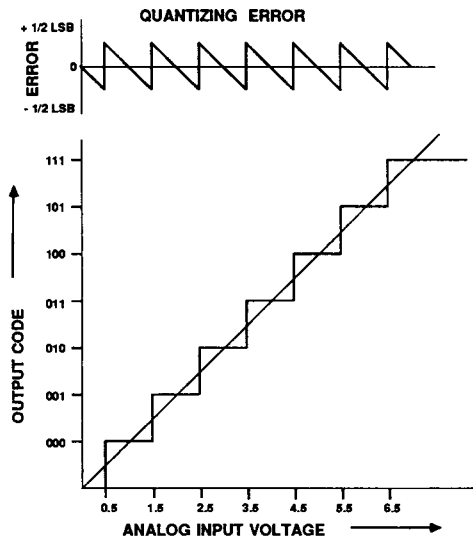
SPT

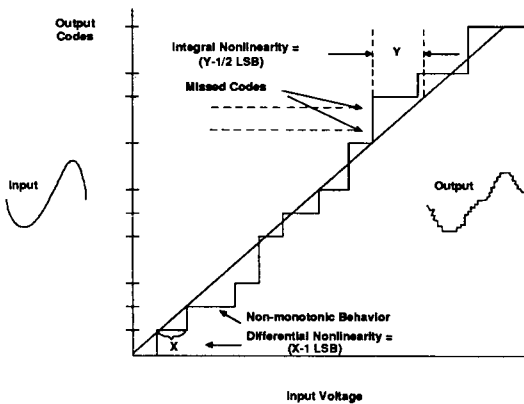**Figure 6 - Quantizing error**

Figure 7 - Dynamic Conditions

THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rated performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC674Z, this is the time delay between the R/C̄ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC674Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HADC674Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC674Z is left-justified. This means that the data represents the analog input as a fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 7 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC674Z is a complete 12-bit Analog-To-Digital converter which consists of a single chip version of the industry standard 674. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample & hold, clock, output buffers and control circuitry to make it possible to use the HADC674Z with few external components.

When the control section of the HADC674Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC674Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with ±15V supplies. If the HADC674Z is used with ±12V supplies, or if external current must be supplied over the full temperature range, an

external buffer amplifier is recommended. Any external load on the HADC674Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC674Z appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the HADC674Z over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC674Z is disconnected from the user's sample and hold. This prevents transients occuring during conversion from being inflicted upon the attached sample and hold buffer. All other 674 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the HADC674Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC674Z acts as any other 674 device because the internal S/H is transparent. The sample/hold function in the HADC674Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HADC674Z and is controlled through the normal $R/\overline{C}$ control line (refer to Figure 8.) When the $R/\overline{C}$ line makes a negative transition, the HADC674Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with

the duration controlled by the internal clock cycle.

During T_{acq}, the equivalent circuit of the HADC674Z in-put is as shown in Figure 9 (the time constant of the input is independant of which input level is used.) This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs., there is more than enough time for settling the input to 12 bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Note that because the sample is taken relative to the $R/\overline{C}$ transition, T_{acq} is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in $T_{acq} = 2.4$ μsecs. ± 0.6 μsecs. between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC674Z.

APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time the actual sample is taken - i.e. the "aperture jitter" or T_{AJ}. The HADC674Z has a nominal aperture jitter of 8 nsecs. between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (See Figure 10). The magnitude of this change for a sine-wave can be calculated:

Assume a sinusoidal signal, maximum slew rate, Sr = $2\pi f Vp$ (Vp = peak voltage, f = frequency of sine wave)
For an N-bit converter to maintain +/- 1/2 LSB accuracy :

Verr $\leq$ Vfs/2^{N+1} (where Verr is the allowable error voltage and Vfs is the full scale voltage)

From Figure 10:

$Sr = \Delta V/ \Delta T = 2\pi f Vp$

Let $\Delta V = $ Verr $= V_{fs}2^{-(N+1)}$, Vp = Vin/2 and $\Delta T = t_{AJ}$ (the time during which unwanted voltage change occurs)

The above conditions then yield:

2

$$Vfs/2^{N+1} \geq \pi f Vin\, t_{AJ} \text{ or } f_{max} \leq Vfs/(\pi Vin\, t_{AJ})2^{N+1}$$

For the HADC674Z, $T_{AJ} = 8$ nsec,
therefore $f_{max} \leq 5KHz$.

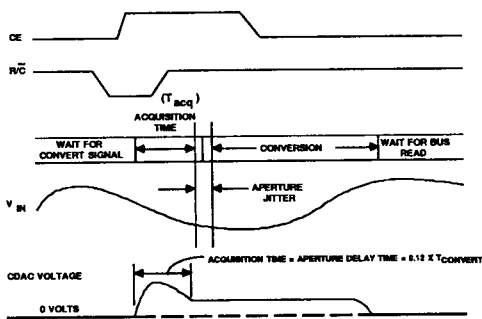For higher frequency signal inputs, an external sample and hold is recommended.
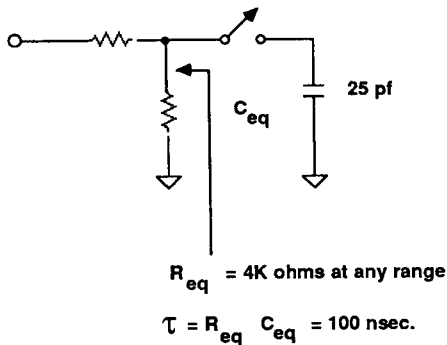
Figure 8 - Sample and Hold Function

R_{eq} = 4K ohms at any range

$\tau = R_{eq}\ C_{eq}$ = 100 nsec.

**Figure 9 - Equivalent HADC674Z
Input Circuit**
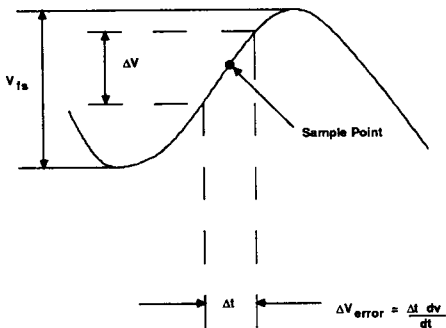
Figure 10 - Aperture Uncertainty

TYPICAL INTERFACE CIRCUIT

The HADC674Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figures 11 and 12. The two typical interface circuits are for operating the HADC674Z in either a unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the P.C. board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC674Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10μF tantalum and a 0.1μF ceramic type in parallel between V_{LOGIC} (pin1) and digital common (pin15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC674Z is being used to upgrade an already existing design.

SPT

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accomodate the ground currents present with this device.

The analog ground current is approximately 6mADC while the digital ground is 3mADC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependant currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC674Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2LSB or +1.22mV for the 10V range and +2.44mV for the 20V range should be applied to the HADC674Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2LSB below the nominal full scale which is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R1 with a 50Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

BIPOLAR

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5V range or to pin 14 for a ±10V range. First apply a DC input voltage 1/2LSB above negative full scale which is -4.9988V for the ±5V range or -9.9976V for the ±10V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2LSB below positive full scale which is +4.9963V for the ±5V range or +9.9927V for the ±10V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

The 100Ω potentiometer R2 provides gain adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (for an LSB of 2.5mV) or 20.48V (for an LSB of 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then to provide gain adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 1000Ω potentiometer in series with pin 14.

CONTROLLING THE HADC674Z

The HADC674Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/C input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/8, CS, A0, R/C and CE). The use of these inputs in controlling the converter's operations is shown in Table 1, and the internal control logic is shown in a simplified schematic in Figure 13.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/C. The other controls must be tied to known states as follows: CE and 12/8 are wired high, A0 and CS are wired low. The output data arrives in words of 12-bits each. The limits on R/C duty cycle are shown in Figures 3 and 4. It may have duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress.

2

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table 1. The latched state determines if the conversion stops with 8-bits (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.
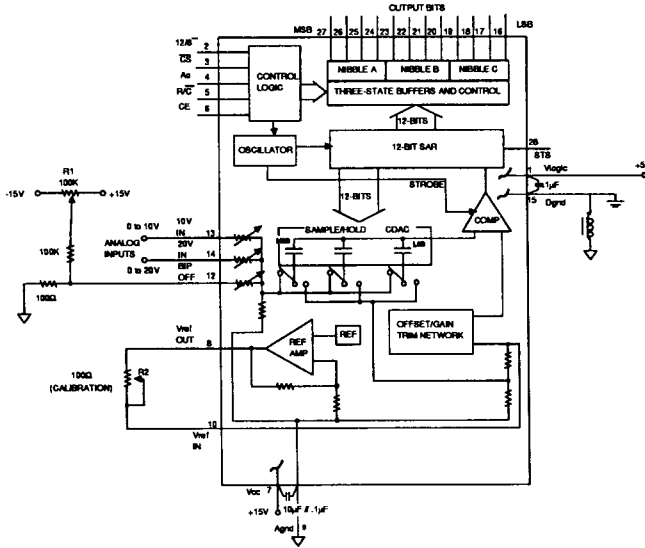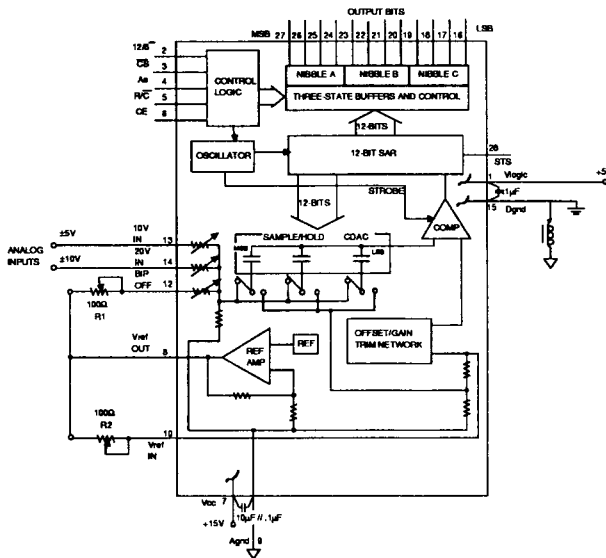

Figure 11 - Unipolar Input Connections

Figure 12 - Bipolar Input Connections
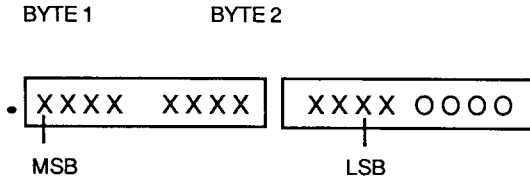
SPT

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new state of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high and $\overline{CS}$ is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible.

Table 1 - Truth Table for the HADC674Z Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:

BYTE 1   BYTE 2

MSB   LSB

This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.
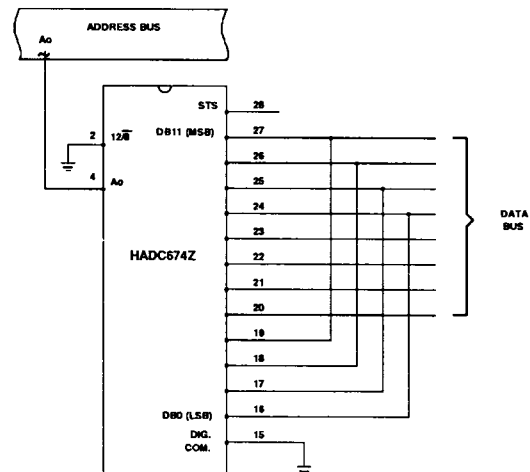

Figure 13 - Interfacing the HADC674Z to an 8-bit Data Bus
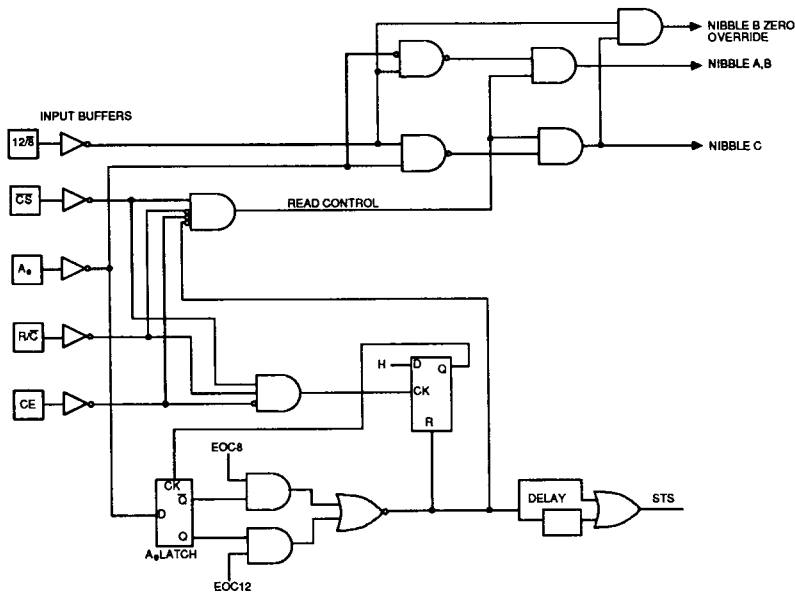
Figure 14 - HADC674Z Control Logic

R₁ - 50Ω,   5%, 1/2 W
R₂ - 1KΩ,   5%, 1/4 W
R₃ - 50Ω,   1%, 1/4 W
R₄ - 10KΩ, 5%, 1/4 W
R₅ - 3.3KΩ, 5%, 1/4 W

C₁ 10µF, 5%
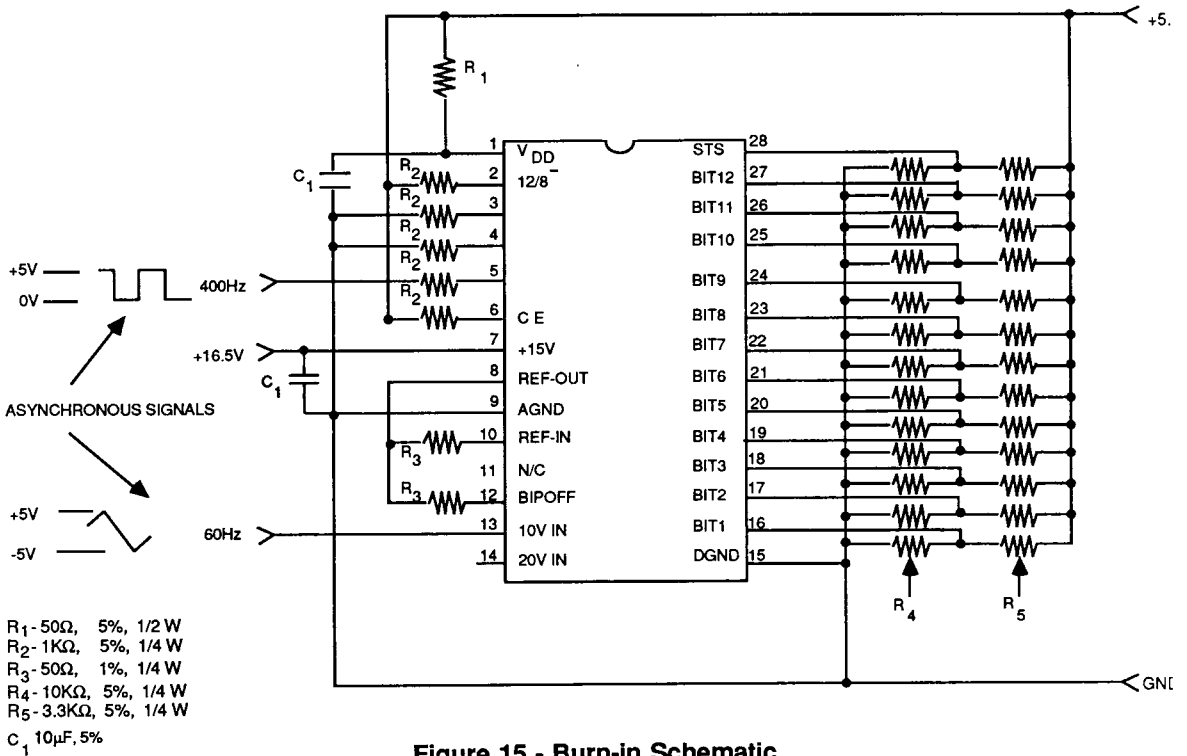
Figure 15 - Burn-in Schematic

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PIN ASSIGNMENT HADC674Z

TOP VIEW

1	VLOGIC	STS	28
2	12/$\overline{8}$	DB11	27
3	$\overline{CS}$	DB10	26
4	Ao	DB9	25
5	R/$\overline{C}$	DB8	24
6	CE	DB7	23
7	VCC	DB6	22
8	REF OUT	DB5	21
9	AGND	DB4	20
10	REF IN	DB3	19
11	N/C (VEE)	DB2	18
12	BIP OFF	DB1	17
13	10V IN	LSB DB0	16
14	20V IN	DGND	15
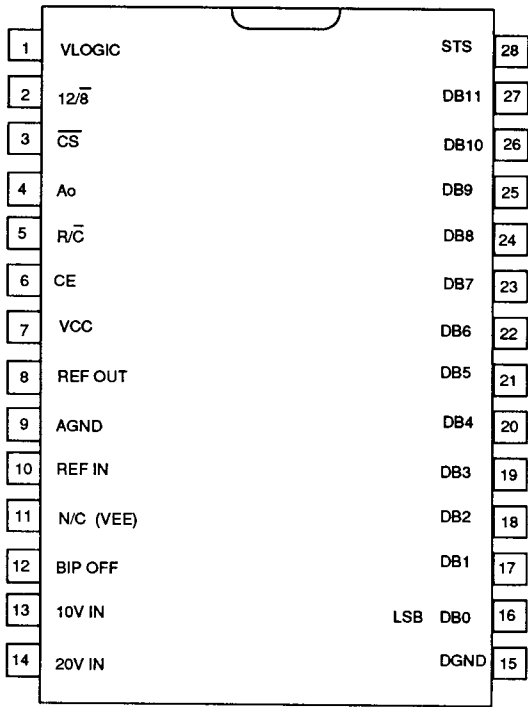
28 LEAD DIP

PIN FUNCTIONS HADC674Z

NAME	FUNCTION
V$_{LOGIC}$	Logic Supply Voltage, Nominally +5V
12/$\overline{8}$	Data Mode Select
$\overline{CS}$	Chip Select
Ao	Byte Address/ Short cycle
R/$\overline{C}$	Read/ Convert
CE	Chip Enable
V$_{CC}$	Analog Positive Supply Voltage Nominally +15V
REF OUT	Reference Output Nominally +10V
AGND	Analog Ground
REF IN	Reference Input
N/C (VEE)	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10V IN	10 Volt Analog Input
20V IN	20V Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

2

*For Ordering Information See Section 1.

SPT