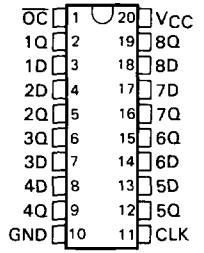
SN54F374, SN74F374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

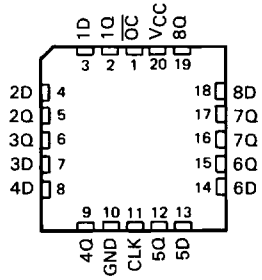
D2932, MARCH 1987

- 8 D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54F374 . . . J PACKAGE
SN74F374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F374 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'F374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

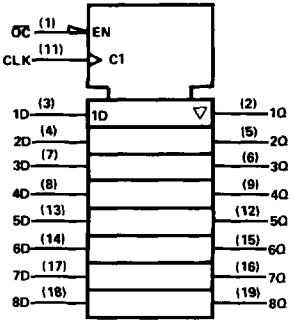
The output control does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54F374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F374 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH FLIP-FLOP)

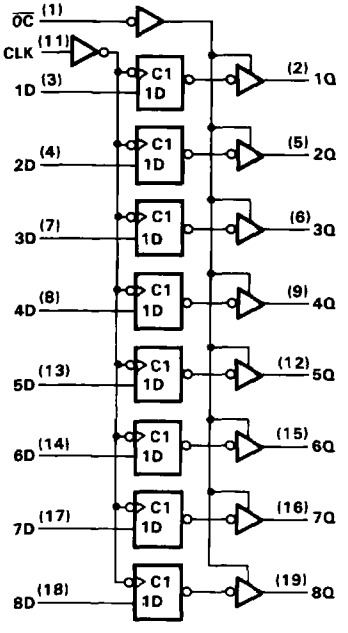
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F374 . . . . . 40 mA
SN74F374 . . . . . 48 mA
Operating free-air temperature range: SN54F374 . . . . . −55°C to 125°C
SN74F374 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F374			SN74F374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F374			SN74F374			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}#	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}¶	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,	See Note 1		55	86		55	86	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
# For the SN74F374 at V_{CC} = 4.75 V and I_{OH} = −1 mA to −3 mA, V_{OH} min = 2.7 V.
NOTE 1: I_{CCZ} is measured with $\overline{OC}$ at 4.5 V and the data inputs grounded.

timing requirements

PARAMETER			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F374		SN54F374		SN74F374		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	60	0	70	MHz
t_{su}	Setup time before CLK↑	Data high	2		2.5		2		ns
		Data low	2		2		2		
t_h	Hold time after CLK↑	Data high	2		2		2		ns
		Data low	2		2.5		2		
t_w	Pulse duration	CLK high	7		7		7		ns
		CLK low	6		6		6		

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F374			SN54F374		SN74F374		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100			60		70		MHz
t_{PLH}	CLK	Q	3.2	6.1	8.5	3.2	10.5	3.2	10	ns
t_{PHL}			3.2	6.1	8.5	3.2	11	3.2	10	
t_{PZH}	$\overline{OC}$	Q	1.2	8.6	11.5	1.2	14	1.2	12.5	ns
t_{PZL}			1.2	5.4	7.5	1.2	10	1.2	8.5	
t_{PHZ}	$\overline{OC}$	Q	1.2	4.9	7	1.2	8	1.2	8	ns
t_{PLZ}			1.2	3.9	5.5	1.2	7.5	1.2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTE 2: See General Information for load circuits and waveforms.

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