

# SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379

## OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

OCTOBER 1976 — REVISED MARCH 1988

- 'LS377 and 'LS378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs
- 'LS379 Contains Four Flip-Flops with Double-Rail Outputs
- Individual Data Input to Each Flip-Flop
- Applications Include:  
Buffer/Storage Registers  
Shift Registers  
Pattern Generators

### description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with an enable input. The 'LS377, 'LS378, and 'LS379 devices are similar to 'LS273, 'LS174, and 'LS175, respectively, but feature a common enable instead of a common clear.

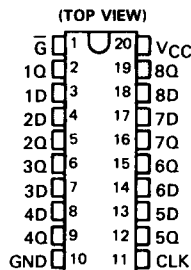
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input  $\bar{G}$  is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the  $\bar{G}$  input.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 MHz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 10 milliwatts per flip-flop.

**FUNCTION TABLE**  
(EACH FLIP-FLOP)

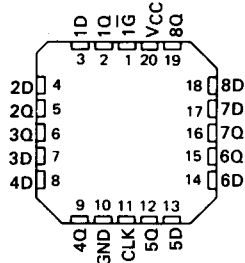
INPUTS			OUTPUTS	
$\bar{G}$	CLOCK	DATA	Q	$\bar{Q}$
H	X	X	$Q_0$	$\bar{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	$Q_0$	$\bar{Q}_0$

SN54LS377 . . . J PACKAGE  
SN74LS377 . . . DW OR N PACKAGE



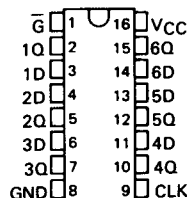
SN54LS377 . . . FK PACKAGE

(TOP VIEW)



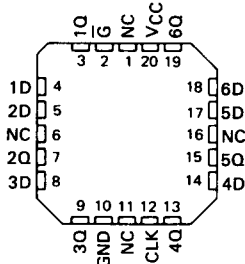
SN54LS378 . . . J OR W PACKAGE  
SN74LS378 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS378 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

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**PRODUCTION DATA** documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

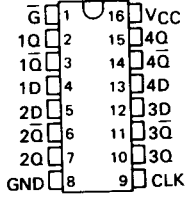
**TEXAS  
INSTRUMENTS**

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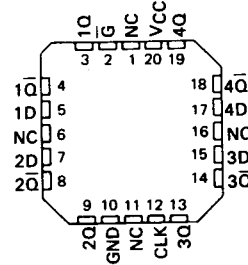
2-895

# SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

SN54LS379 . . . J OR W PACKAGE  
SN74LS379 . . . D OR N PACKAGE  
(TOP VIEW)



SN54LS379 . . . FK PACKAGE  
(TOP VIEW)

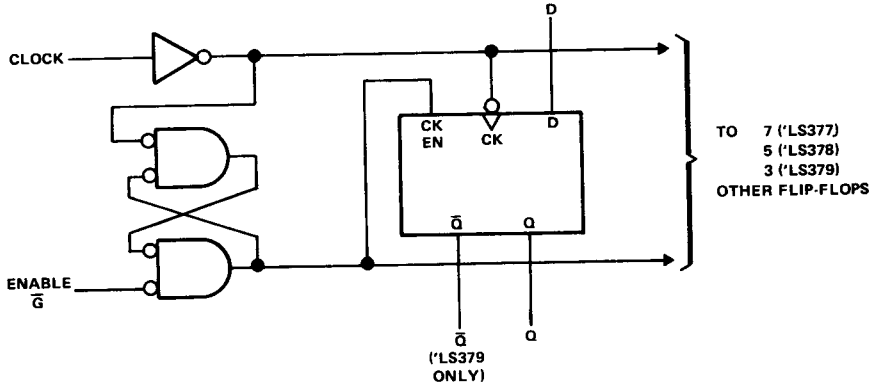


NC - No internal connection

2

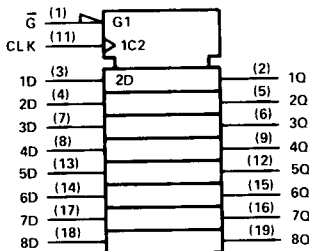
logic diagram (positive logic)

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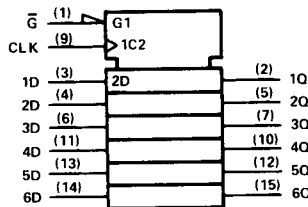


logic symbols†

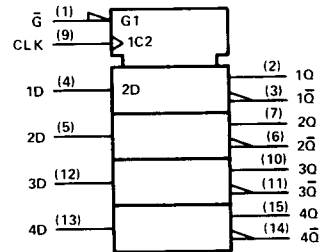
'LS377



'LS378



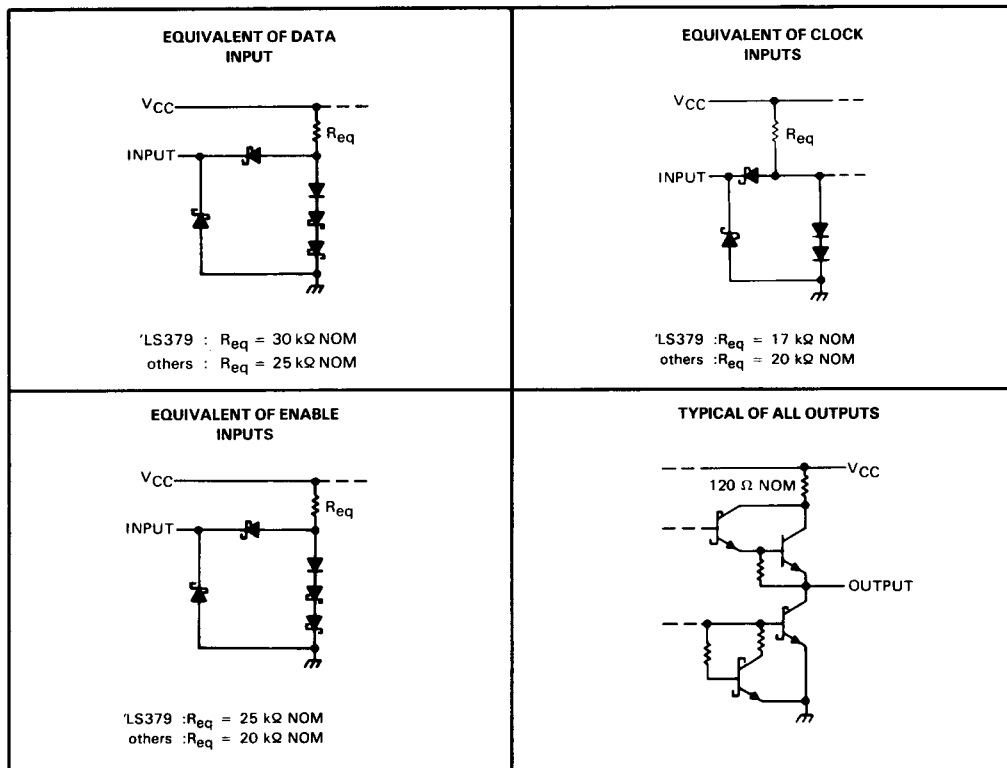
'LS379



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

**SN54LS377, SN54LS378, SN54LS379,  
SN74LS377, SN74LS378, SN74LS379**  
**OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE**

schematics of inputs and outputs



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**absolute maximum rating over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS*	-55°C to 125°C
SN74LS*	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**SN54LS377, SN54LS378, SN54LS379,  
SN74LS377, SN74LS378, SN74LS379  
OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE**

**recommended operating conditions**

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I <sub>OH</sub>	-400			-400			μA
Low-level output current, I <sub>OL</sub>	4			8			mA
Clock frequency, f <sub>clock</sub>	0	30		0	30		MHz
Width of clock pulse, t <sub>w</sub>	20			20			ns
Setup time, t <sub>su</sub>	Data input			20†			ns
	Enable active-state			25†			
	Enable inactive-state			10†			
Hold time, t <sub>h</sub>	5†			5†			ns
Operating free-air temperature, T <sub>A</sub>	-55	125		0	70		°C

† The arrow indicates that the rising edge of the clock pulse is used for reference.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

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PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage		0.7			0.8			V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5			-1.5			V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 μA	2.5	3.5		2.7	3.5		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 4 mA 0.25 0.4		I <sub>OL</sub> = 8 mA 0.25 0.4		0.35 0.5		V
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V	0.1			0.1			mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	20			20			μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-0.4			-0.4			mA
I <sub>OS</sub> Short-circuit output current§	V <sub>CC</sub> = MAX	-20	-100		-20	-100		mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 2	'LS377			17 28			mA
		'LS378			13 22			mA
		'LS379			9 15			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Note more than one input should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and ground applied to all data and enable inputs, I<sub>CC</sub> is measured after a momentary ground, then 4.5 V, is applied to clock.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub> Maximum clock frequency	C <sub>L</sub> = 15 pF,	30	40		MHz
t <sub>PLH</sub> Propagation delay time, low-to-high-level output from clock	R <sub>L</sub> = 2 kΩ		17	27	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output from clock	See Note 3		18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.