TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74LCX74F, TC74LCX74FN, TC74LCX74FT

## LOW VOLTAGE DUAL D-TYPE FLIP FLOP WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX74 is a high performance CMOS D-TYPE FLIP FLOP. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) $V_{CC}$ applications, but it could be used to interface to 5V supply environment for inputs.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.

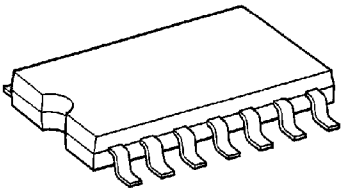
All inputs are equipped with protection circuits against static discharge.

### FEATURES

- Low voltage operation : $V_{CC} = 2.0 \sim 3.6V$
- High speed operation : $t_{pd} = 7.0ns$ (Max.) ($V_{CC} = 3.0 \sim 3.6V$)
- Output current : $|I_{OH}| / I_{OL} = 24mA$ (Min.) ($V_{CC} = 3.0V$)
- Latch-up performance : $\pm 500mA$
- Available in JEDEC SOP, EIAJ SOP and TSSOP
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC / VHC / HC / F / ALS / LS etc.) 74 type.

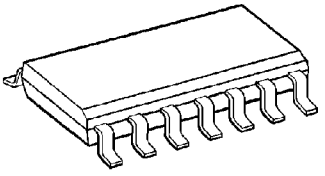
(Note) The JEDEC SOP (FN) is not available in Japan.

TC74LCX74F



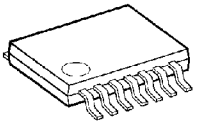
SOP14-P-300-1.27

TC74LCX74FN



SOL14-P-150-1.27

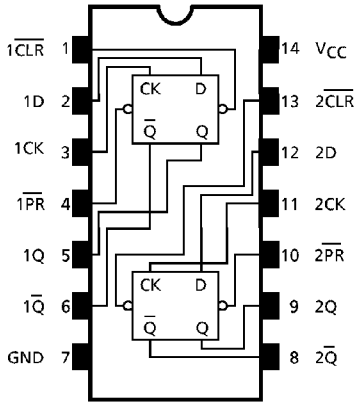
TC74LCX74FT



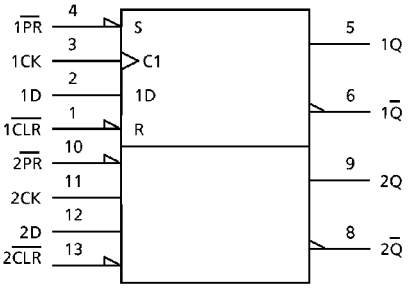
TSSOP14-P-0044-0.65

Weight
SOP14-P-300-1.27 : 0.18g (Typ.)
SOL14-P-150-1.27 : 0.12g (Typ.)
TSSOP14-P-0044-0.65 : 0.06g (Typ.)

## PIN ASSIGNMENT




## IEC LOGIC SYMBOL




## TRUTH TABLE

| INPUTS | | | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{PR}$ | D | CK | Q | $\overline{Q}$ | |
| L | H | X | X | L | H | CLEAR |
| H | L | X | X | H | L | PRESET |
| L | L | X | X | H | H | — |
| H | H | L | ↑ | L | H | — |
| H | H | H | ↑ | H | L | — |
| H | H | X | ↓ | $Q_n$ | $\overline{Q}_n$ | NO CHANGE |

X : Don't care

## MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | −0.5~7.0 | V |
| DC Input Voltage | $V_{IN}$ | −0.5~7.0 | V |
| DC Output Voltage | $V_{OUT}$ | −0.5~7.0 (Note 1) | V |
| | | −0.5~$V_{CC}$+0.5 (Note 2) | |
| Input Diode Current | $I_{IK}$ | −50 | mA |
| Output Diode Current | $I_{OK}$ | ±50 (Note 3) | mA |
| DC Output Current | $I_{OUT}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 180 | mW |
| DC $V_{CC}$/Ground Current | $I_{CC}$/$I_{GND}$ | ±100 | mA |
| Storage Temperature | $T_{stg}$ | −65~150 | °C |

(Note 1) VCC = 0V
(Note 2) High or Low State. $I_{OUT}$ absolute maximum rating must be observed.
(Note 3) $V_{OUT}$<GND, $V_{OUT}$>$V_{CC}$

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**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2.0~3.6 | V |
| | | 1.5~3.6 (Note 4) | |
| Input Voltage | $V_{IN}$ | 0~5.5 | V |
| Output Voltage | $V_{OUT}$ | 0~5.5 (Note 5) | V |
| | | 0~ $V_{CC}$ (Note 6) | |
| Output Current | $I_{OH}$ / $I_{OL}$ | ±24 (Note 7) | mA |
| | | ±12 (Note 8) | |
| Operating Temperature | $T_{opr}$ | −40~85 | °C |
| Input Rise And Fall Time | dt / dv | 0~10 (Note 9) | ns / V |

(Note 4) Data Retention Only
(Note 5) VCC = 0V
(Note 6) High or Low State
(Note 7) $V_{CC}$ = 3.0~3.6V
(Note 8) $V_{CC}$ = 2.7~3.0V
(Note 9) $V_{IN}$ = 0.8~2.0V, $V_{CC}$ = 3.0V

**ELECTRICAL CHARACTERISTICS**

DC characteristics (Ta = −40~85°C)

| PARAMETER | | SYMBOL | TEST CONDITION | | $V_{CC}$ (V) | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| Input Voltage | "H" Level | $V_{IH}$ | | | 2.7~3.6 | 2.0 | — | V |
| | "L" Level | $V_{IL}$ | | | 2.7~3.6 | — | 0.8 | |
| Output Voltage | "H" Level | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −100μA | 2.7~3.6 | $V_{CC}$ −0.2 | — | V |
| | | | | $I_{OH}$ = −12mA | 2.7 | 2.2 | — | |
| | | | | $I_{OH}$ = −18mA | 3.0 | 2.4 | — | |
| | | | | $I_{OH}$ = −24mA | 3.0 | 2.2 | — | |
| | "L" Level | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 100μA | 2.7~3.6 | — | 0.2 | |
| | | | | $I_{OL}$ = 12mA | 2.7 | — | 0.4 | |
| | | | | $I_{OL}$ = 16mA | 3.0 | — | 0.4 | |
| | | | | $I_{OL}$ = 24mA | 3.0 | — | 0.55 | |
| Input Leakage Current | | $I_{IN}$ | $V_{IN}$ = 0~5.5V | | 2.7~3.6 | — | ±5.0 | μA |
| Power Off Leakage Cuurent | | $I_{OFF}$ | $V_{IN}$ / $V_{OUT}$ = 5.5V | | 0 | — | 10.0 | μA |
| Quiescent Supply Current | | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 2.7~3.6 | — | 10.0 | μA |
| | | | $V_{IN}$ / $V_{OUT}$ = 3.6~5.5V | | 2.7~3.6 | — | ±10.0 | |
| Quiescent In $I_{CC}$ Per Input | | $\Delta I_{CC}$ | $V_{IH}$ = $V_{CC}$ − 0.6V | | 2.7~3.6 | — | 500 | μA |

AC characteristics (Ta = – 40~85°C)

| PARAMETER | SYMBOL | TEST CONDITION | $V_{CC}$ (V) | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Maximam Clock Frequency | $f_{MAX}$ | (Fig.1, 2) | 2.7 | — | — | MHz |
| | | | 3.3 ± 0.3 | 150 | — | |
| Propagation Delay Time (CK-Q, $\overline{Q}$) | $t_{pLH}$ $t_{pHL}$ | (Fig.1, 2) | 2.7 | — | 8.0 | ns |
| | | | 3.3 ± 0.3 | 1.5 | 7.0 | |
| Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$) | $t_{pLH}$ $t_{pHL}$ | (Fig.1, 4) | 2.7 | — | 8.0 | ns |
| | | | 3.3 ± 0.3 | 1.5 | 7.0 | |
| Minimum Pulse Width (CK) | $t_{W}$ (H) $t_{W}$ (L) | (Fig.1, 2, 3) | 2.7 | 3.3 | — | ns |
| | | | 3.3 ± 0.3 | 3.3 | — | |
| Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$) | $t_{W}$ (L) | (Fig.1, 2, 3) | 2.7 | 3.6 | — | ns |
| | | | 3.3 ± 0.3 | 3.3 | — | |
| Minimum Set-up Time | $t_s$ | (Fig.1, 2) | 2.7 | 2.5 | — | ns |
| | | | 3.3 ± 0.3 | 2.5 | — | |
| Minimum Hold Time | $t_h$ | (Fig.1, 2) | 2.7 | 1.5 | — | ns |
| | | | 3.3 ± 0.3 | 1.5 | — | |
| Minimum Removal Time | $t_{rem}$ | (Fig.1, 3) | 2.7 | 3.0 | — | ns |
| | | | 3.3 ± 0.3 | 2.5 | — | |
| Output To Output Skew | $t_{osLH}$ $t_{osHL}$ | (Note 10) | 2.7 | — | — | ns |
| | | | 3.3 ± 0.3 | — | 1.0 | |

(Note 10) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

**DYNAMIC SWITCHING CHARACTERISTICS** (Ta = 25°C, Input $t_r = t_f = 2.5$ns, $C_L = 50$pF, $R_L = 500\Omega$)

| PARAMETER | SYMBOL | TEST CONDITION | $V_{CC}$ (V) | TYP. | UNIT |
|---|---|---|---|---|---|
| Quiet Output Maximum Dynamic $V_{OL}$ | $V_{OLP}$ | $V_{IH}$ = 3.3V, $V_{IL}$ = 0V | 3.3 | 0.8 | V |
| Quiet Output Minimum Dynamic $V_{OL}$ | $\|V_{OLV}\|$ | $V_{IH}$ = 3.3V, $V_{IL}$ = 0V | 3.3 | 0.8 | V |

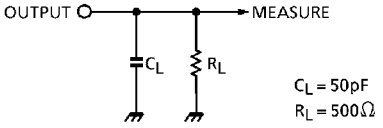
**CAPACITIVE CHARACTERISTICS** (Ta = 25°C)

| PARAMETER | SYMBOL | TEST CONDITION | $V_{CC}$ (V) | TYP | UNIT |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | — | 3.3 | 7 | pF |
| Output Capacitance | $C_{OUT}$ | | 0 | 8 | pF |
| Power Dissipation Capacitance | $C_{PD}$ | $f_{IN}$ = 10MHz (Note 11) | 3.3 | 25 | pF |

(Note 11) $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :
$I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2$ (per F / F)

## TEST CIRCUIT

Fig.1




## AC WAVEFORM

Fig.2 $t_{pLH}$, $t_{pHL}$, $t_W$, $t_s$, $t_h$

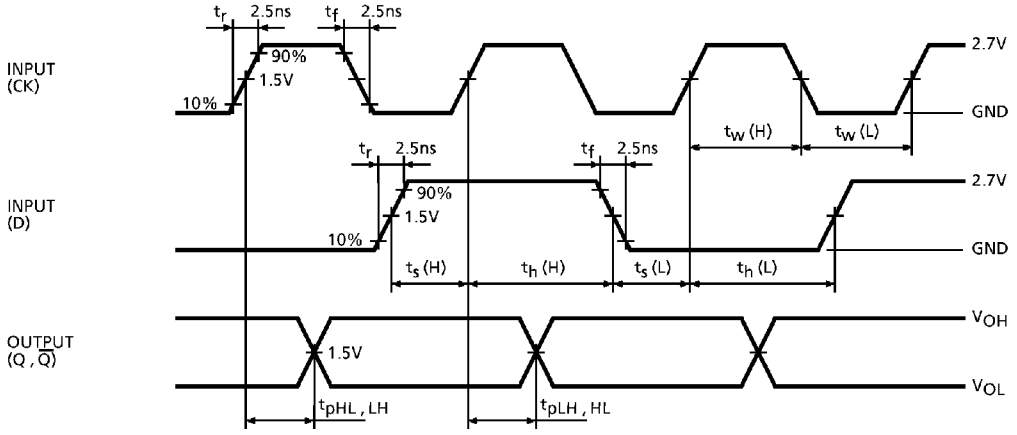



Fig.3 $t_{rem}$

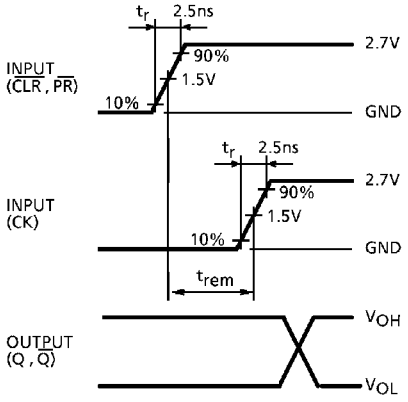
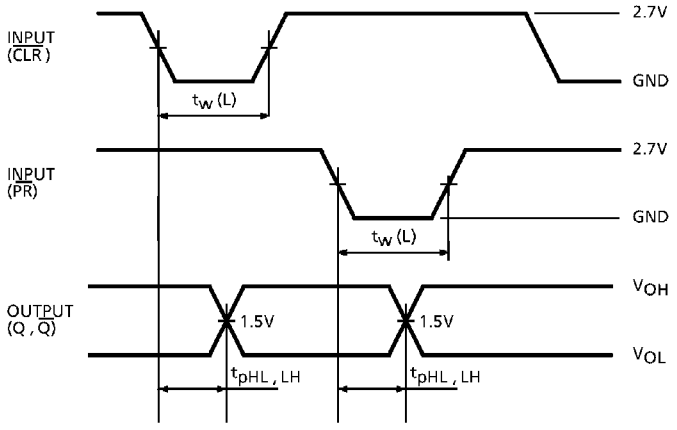


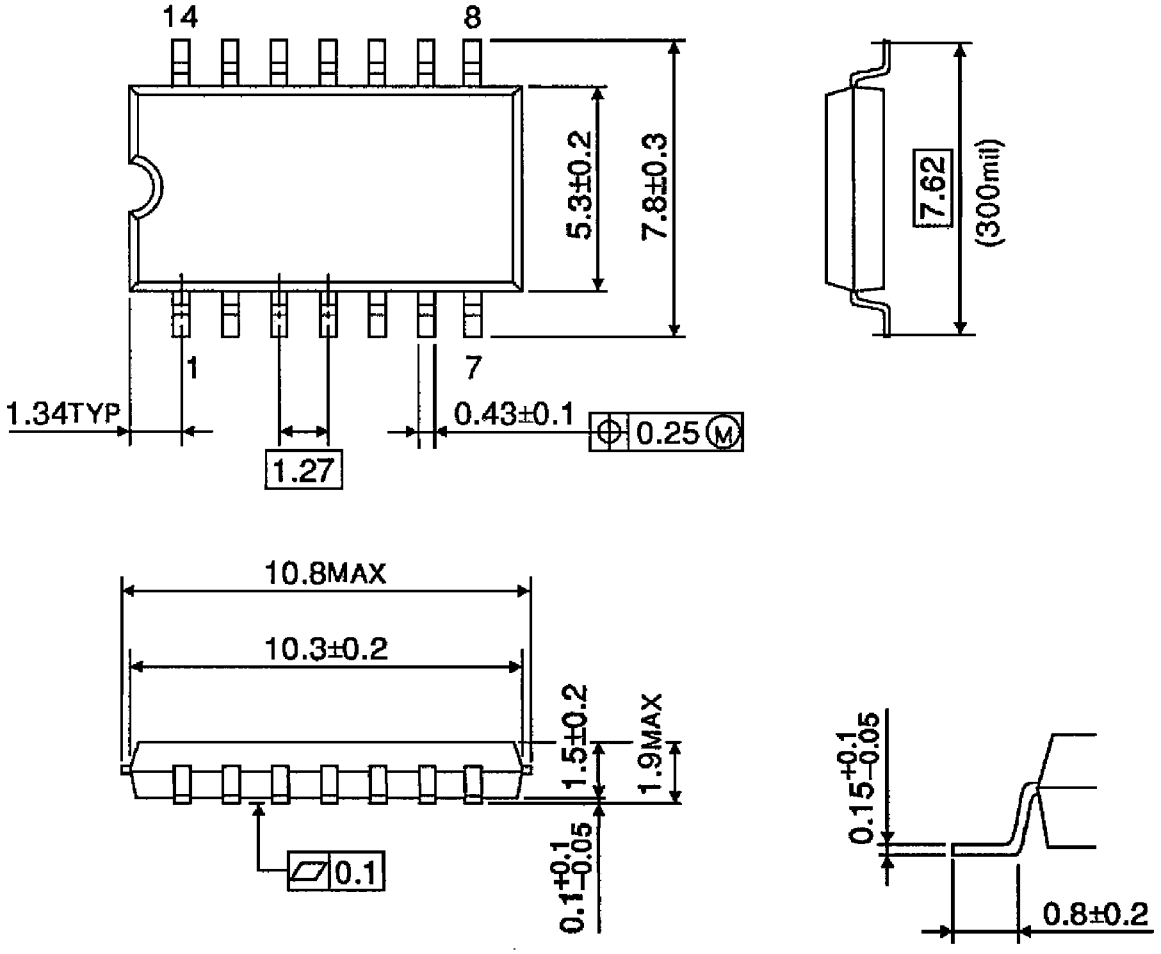

Fig.4 $t_{pLH}$, $t_{pHL}$



**OUTLINE DRAWING**

SOP14-P-300-1.27

Unit : mm



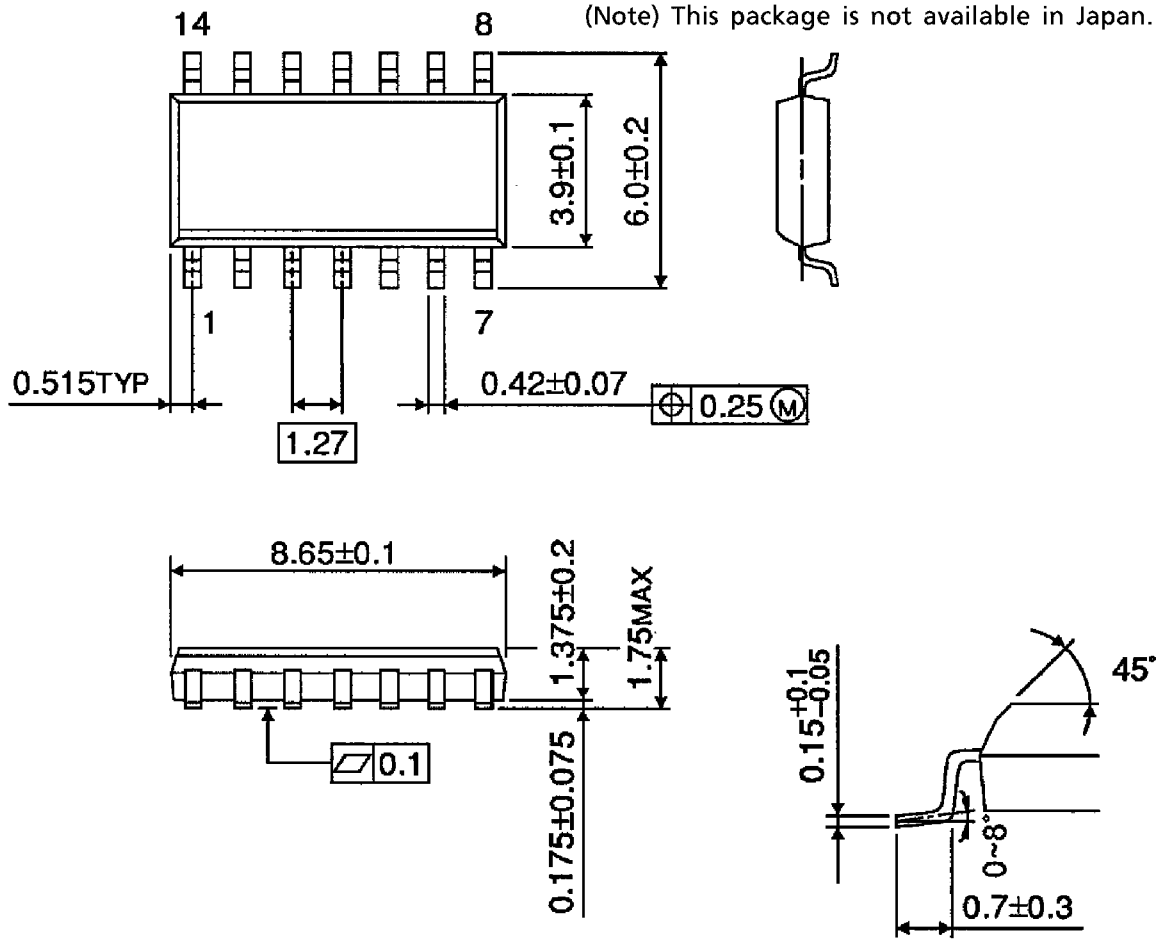

Weight : 0.18g (Typ.)

**OUTLINE DRAWING**

SOL14-P-150-1.27

Unit : mm

(Note) This package is not available in Japan.

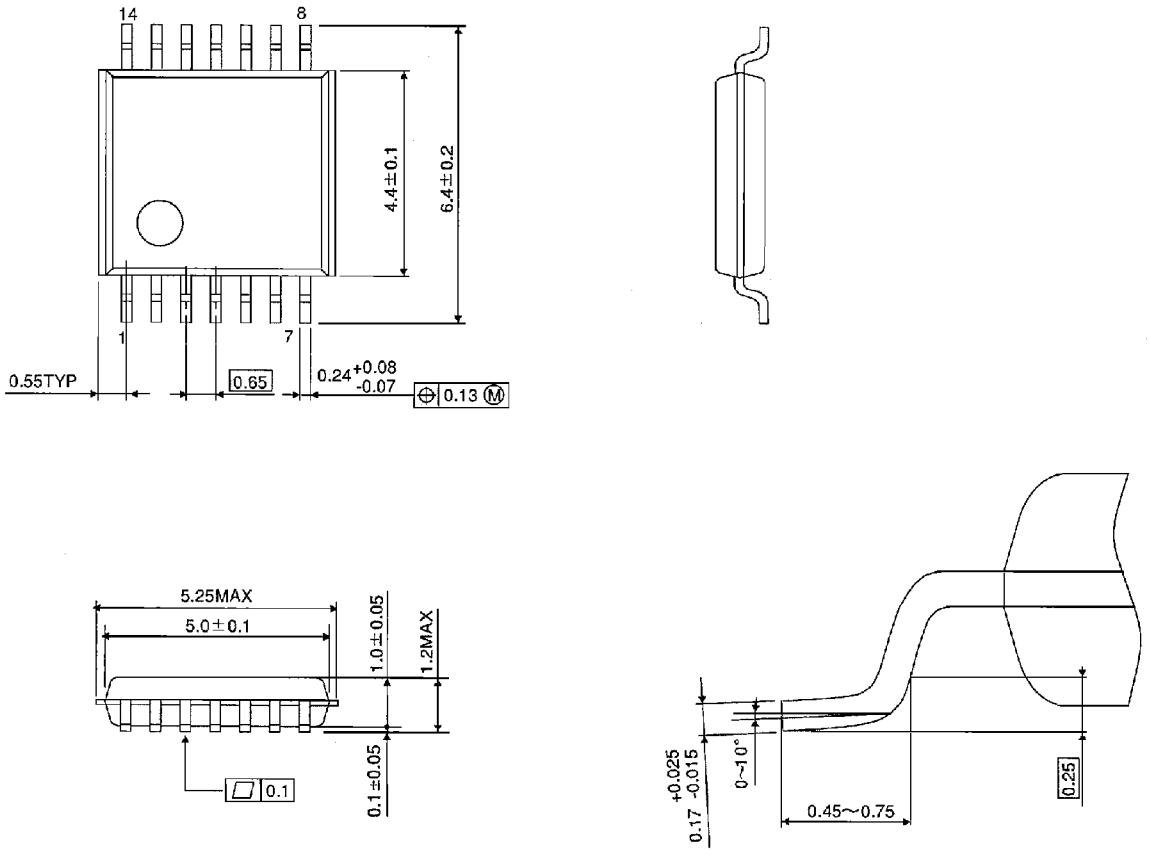



Weight : 0.12g (Typ.)

**OUTLINE DRAWING**

TSSOP14-P-0044-0.65

Unit : mm




Weight : 0.06g (Typ.)