HD74AC259/HD74ACT259 • 8-Bit Addressable Latch

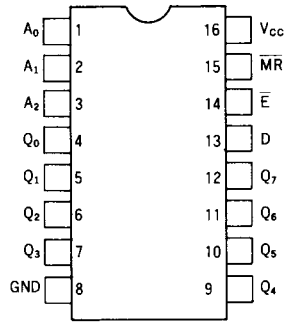
Description

The 'AC259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable or storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable.

Features

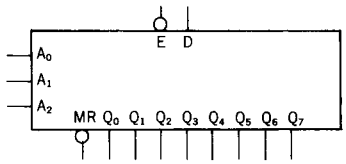
- Serial-to-Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random(Addressable)Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear
- Output Source/Sink 24mA
- HD74ACT259 has TTL Compatible Inputs

Pin Assignment



(Top View)

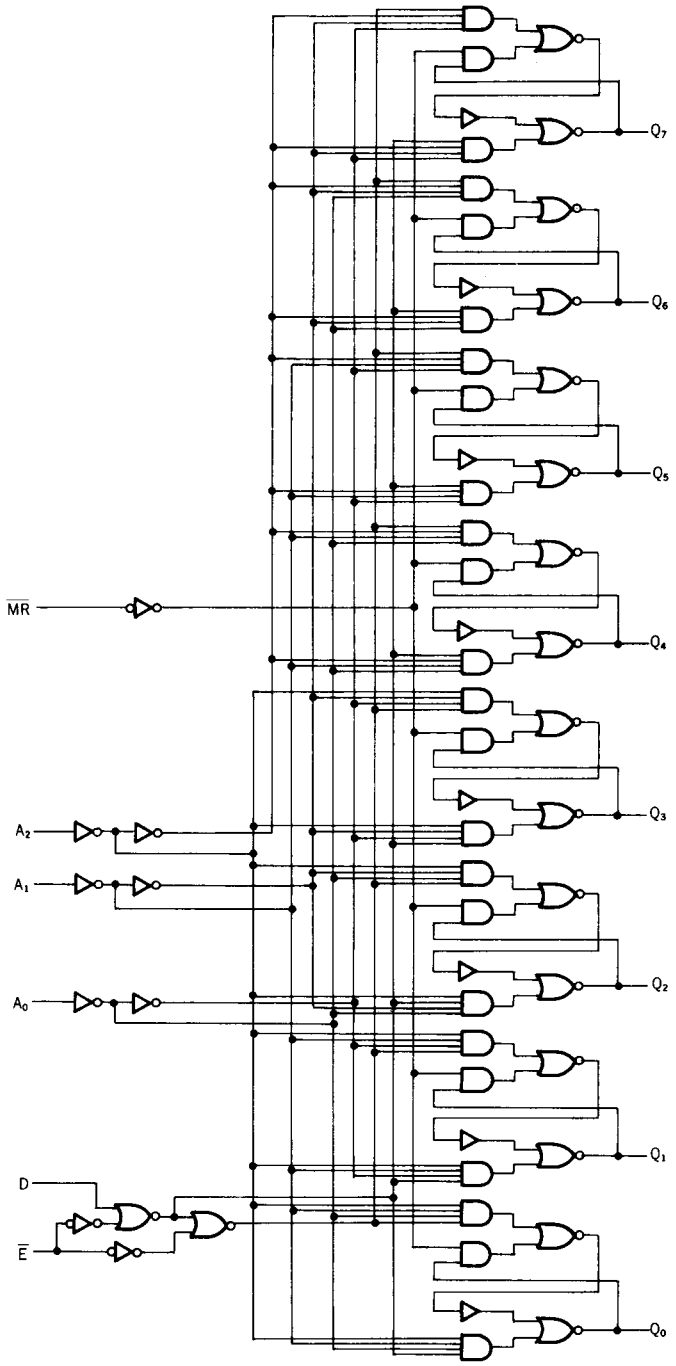
Logic Symbol



Pin Names

A_0—A_2	Adress Inputs
$\overline{D}$	Data Inputs
$\overline{E}$	Enable Input(Active LOW)
$\overline{MR}$	Master Reset(Active LOW)
Q_0—Q_7	Latch Outpzts

Logic Diagram



Function Table

Operating Mode	Inputs						Outputs							
	$\overline{MR}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (Do Nothing)	H	H	X	X	X	X	q0	q1	q2	q3	q4	q5	q6	q7
Addressable Latch	H	L	d	L	L	L	Q=d	q1	q2	q3	q4	q5	q6	q7
	H	L	d	H	L	L	q0	Q=d	q2	q3	q4	q5	q6	q7
	H	L	d	L	H	L	q0	q1	Q=d	q3	q4	q5	q6	q7
	H	L	d	H	H	L	q0	q1	q2	Q=d	q4	q5	q6	q7
	H	L	d	L	L	H	q0	q1	q2	q3	Q=d	q5	q6	q7
	H	L	d	H	L	H	q0	q1	q2	q3	q4	Q=d	q6	q7
	H	L	d	L	H	H	q0	q1	q2	q3	q4	q5	Q=d	q7
	H	L	d	H	H	H	q0	q1	q2	q3	q4	q5	q6	Q=d

H : High Voltage Level
L : Low Voltage Level
X : Immaterial
d : High or Low data one setup time prior to the Low-to-High Enable transition.
q : Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

DC Characteristics(unless oterwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5V$, Ta=Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5V$, Ta=25℃
I_{CCT}	Maximum I_{CC}/Input (HD74ACT259)	1.5	mA	$V_{IN}=V_{CC}-2.1V$, $V_{CC}=5.5V$, Ta=Worst Case

AC Characteristics:HD74AC259

Symbol	Paramater	V_{CC}* (V)	Ta=25℃ C_L=50pF			Ta=−40℃ to +85℃ C_L=50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	65 110			60 95		MHz
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn	3.3 5.0	1.0 1.0	8.5 6.5	14.5 9.0	1.0 1.0	16.5 10.5	ns
t_{PLH}	Propagation Delay Dn to Qn	3.3 5.0	1.0 1.0	7.0 5.5	10.5 7.5	1.0 1.0	12.0 8.5	ns
t_{PHL}	Propagation Delay Dn to Qn	3.3 5.0	1.0 1.0	7.0 5.5	10.5 7.5	1.0 1.0	12.0 8.5	ns
t_{PLH}	Propagation Delay An to Qn	3.3 5.0	1.0 1.0	11.5 8.0	18.5 11.5	1.0 1.0	21.5 14.0	ns
t_{PHL}	Propagation Delay An to Qn	3.3 5.0	1.0 1.0	11.5 8.0	18.5 11.5	1.0 1.0	21.0 13.5	ns
t_{PLH}	Propagation Delay $\overline{E}$ to Q	3.3 5.0	1.0 1.0	9.0 6.5	15.0 9.0	1.0 1.0	17.0 10.5	ns
t_{PHL}	Propagation Delay $\overline{E}$ to Qn	3.3 5.0	1.0 1.0	9.0 6.5	14.0 8.5	1.0 1.0	16.0 10.0	ns

* Voltage Range 3.3 is 3.0V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements:HD74AC259

Symol	Parameter	Vcc* (V)	Ta=+25℃ C_L=50pF		Ta=−40℃ to +85℃ C_L=50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time HIGH or LOW D to $\overline{E}$	3.3 5.0	1.0 0.0	3.5 3.0	3.5 3.0	ns
t_h	Hold Time, HIGH or LOW D to $\overline{E}$	3.3 5.0	0.5 0.5	2.0 2.0	2.0 2.0	ns
t_{su}	Setup Time, HIGH or LOW An to $\overline{E}$	3.3 5.0	1.0 0.0	6.0 4.5	7.0 5.0	ns
t_h	Hold Time, HIGH or LOW An to $\overline{E}$	3.3 5.0	−3.0 −1.0	0.0 0.0	0.0 0.0	ns
t_w	Pulse width	3.3 5.0	3.0 3.0	5.5 4.5	7.0 5.0	ns

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT259 Preliminary

Symbol	Parameter	Vcc* (V)	Ta = +25°C, C_L = 50pF			Ta = -40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock Frequency	5.0	70			60		MHz
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn	5.0	1.0		10.0	1.0	11.5	ns
t_{PLH}	Propagation Delay $\overline{Dn}$ to Qn	5.0	1.0		9.5	1.0	10.5	ns
t_{PHL}	Propagation Delay $\overline{Dn}$ to Qn	5.0	1.0		9.5	1.0	10.5	ns
t_{PLH}	Propagation Delay An to Qn	5.0	1.0		12.5	1.0	15.0	ns
t_{PHL}	Propagation Delay An to Qn	5.0	1.0		12.5	1.0	15.0	ns
t_{PLH}	Propagation Delay $\overline{E}$ to Q	5.0	1.0		11.0	1.0	12.5	ns
t_{PHL}	Propagation Delay $\overline{E}$ to Q	5.0	1.0		10.5	1.0	12.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74ACT259 Preliminary

Symbol	Parameter	Vcc* (V)	Ta = +25°C, C_L = 50pF	Ta = −40°C to +85°C, C_L = 50pF	Unit
			Typ	Guaranteed Minimum	
t_{su}	Setup Time, HIGH or LOW D to $\overline{E}$	5.0		4.0	4.0	ns
t_h	Hold Time, HIGH or LOW D to $\overline{E}$	5.0		2.5	2.5	ns
t_{su}	Setup Time, HIGH or LOW An $\overline{E}$	5.0		4.5	5.0	ns
t_h	Hold Time, HIGH or LOW An to $\overline{E}$	5.0		1.5	1.5	ns
t_w	Pulse width HIGH or LOW	5.0		7.0	8.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5 V
C_{PD}	Power Dissipation Capacitance	3.5	pF	V_{CC} = 5.0 V