Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT 54/74FCT821A/B-
IDT 54/74FCT826A/B*

FEATURES:

- Equivalent to AMD's Am29821-26 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel registers with positive edge-triggered D-type flip-flops
  - Non-inverting CP-Y t_{PD} = 7.5ns typ.
  - Inverting CP-Y t_{PD} = 7.5ns typ.
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- I_{OL} = 48mA (commercial), 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

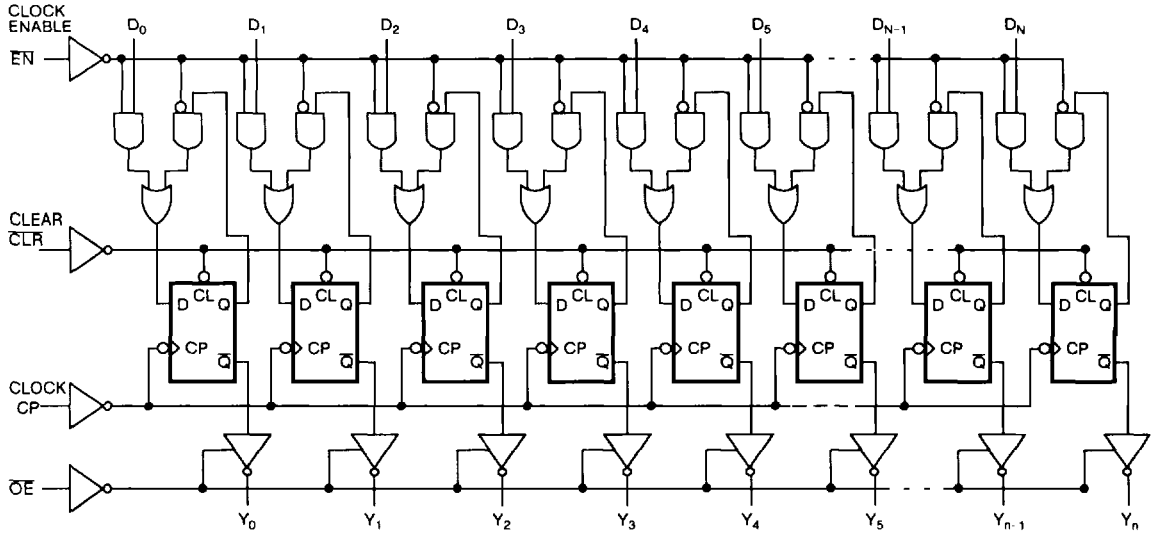
DESCRIPTION:

The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821 and IDT54/74FCT822 are buffered, 10-bit wide versions of the popular '374/'534 functions. The IDT54/74FCT823 and IDT54/74FCT824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825 and IDT54/74FCT826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

	DEVICE		
	10-BIT	9-BIT	8-BIT
Non-inverting	54/74FCT821A/B	54/74FCT823A/B	54/74FCT825A/B
Inverting	54/74FCT822A/B	54/74FCT824A/B	54/74FCT826A/B

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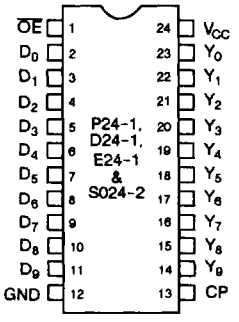
*Advance information only for IDT54/74FCT822 and IDT54/74FCT826.

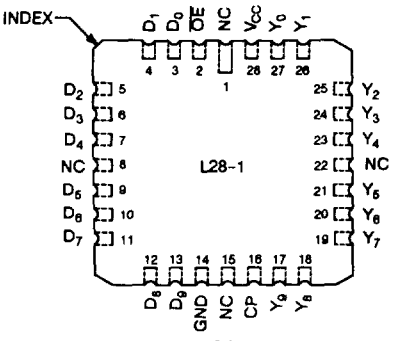
PIN CONFIGURATIONS

LOGIC SYMBOLS

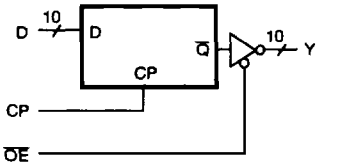
IDT54/74FCT821/IDT54/74FCT822 10-BIT REGISTERS



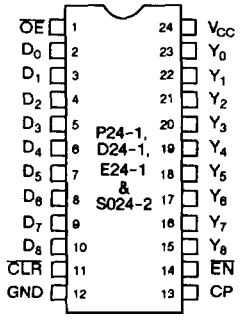
DIP/CERPACK/SOIC
TOP VIEW



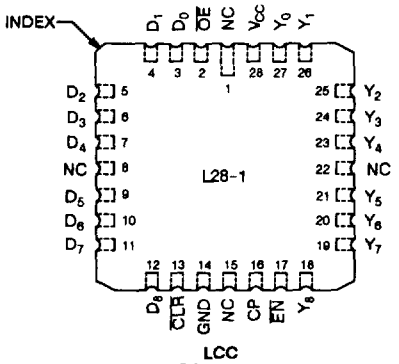
LCC
TOP VIEW



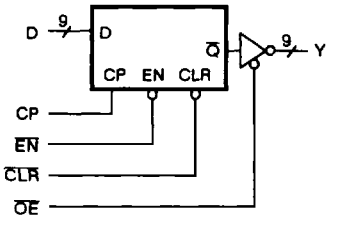
IDT54/74FCT823/IDT54/74FCT824 9-BIT REGISTERS



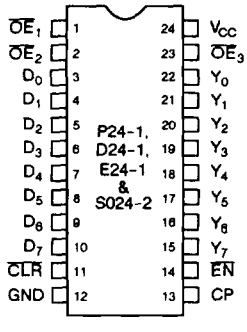
DIP/CERPACK/SOIC
TOP VIEW



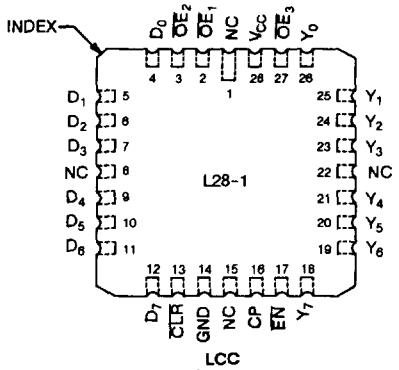
LCC
TOP VIEW



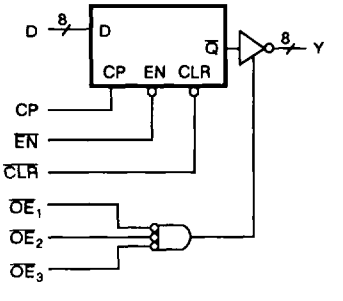
IDT54/74FCT825/IDT54/74FCT826 8-BIT REGISTERS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



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PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D_I	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I, $\overline{Y}_I$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

FUNCTION TABLES [1]
IDT54/74FCT821/23/25

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	
H	X	L	L	↑	L	Z	High Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

FUNCTION TABLES [1]
IDT54/74FCT822/24/26

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	
H	X	L	L	↑	H	Z	High Z
H	X	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

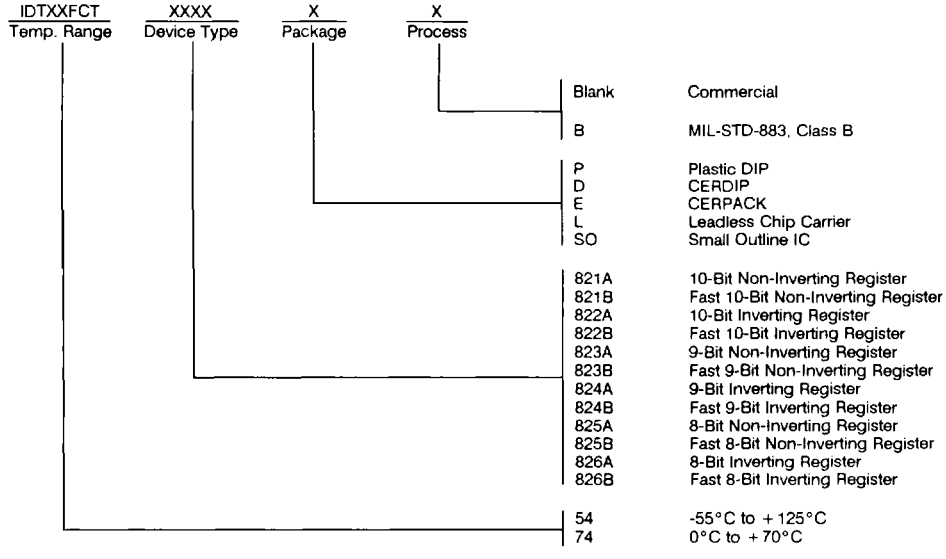
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	IDT54/74FCT821A-26A				IDT54/74FCT821B-26B				UNIT
			COM'L.		MIL.		COM'L.		MIL.		
			MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	–	10	–	11.5	–	7.5	–	8.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	20	–	20	–	15	–	16	ns
t_{SU}	Data to CP Set-up Time	C_L = 50pF R_L = 500Ω	4	–	4	–	3	–	3	–	ns
t_H	Data CP Hold Time		2	–	2	–	1.5	–	1.5	–	ns
t_{SU}	Enable ($\overline{EN}$ ↓) to CP Set-up Time		4	–	4	–	3.0	–	3.0	–	ns
t_{SU}	Enable ($\overline{EN}$ ↓) to CP Set-up Time		4	–	4	–	3.0	–	3.0	–	ns
t_H	Enable ($\overline{EN}$) Hold Time		2	–	2	–	0	–	0	–	ns
t_{PHL}	Propagation Delay, Clear to Y_i		–	14	–	15	–	9.0	–	9.5	ns
t_{SU}	Clear Recovery ($\overline{CLR}$ ↓) Time		6	–	7	–	6.0	–	6.0	–	ns
t_{PWH}	Clock Pulse Width HIGH		7	–	7	–	6.0	–	6.0	–	ns
t_{PWL}	Clock Pulse Width LOW		7	–	7	–	6.0	–	6.0	–	ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width		6	–	7	–	6.0	–	6.0	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ ↓ to Y_i	C_L = 50pF R_L = 500Ω	–	12	–	13	–	8	–	9	ns
t_{PZH} t_{PZL}		C_L = 300pF[3] R_L = 500Ω	–	23	–	25	–	15	–	16	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i	C_L = 5pF[3] R_L = 500Ω	–	9	–	10	–	6.5	–	7	ns
t_{PHZ} t_{PLZ}		C_L = 50pF R_L = 500Ω	–	8	–	9	–	7.5	–	8	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

ORDERING INFORMATION



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