National Semiconductor

74BCT541
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'BCT541 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. This device is functionally similar to the 'BCT244 but has a broadside pinout.

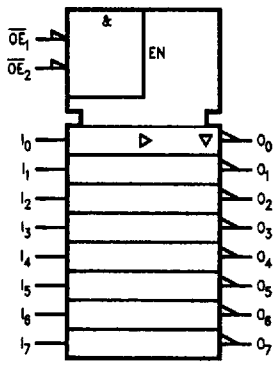
Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Low I_{CCZ} through BiCMOS techniques
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbol

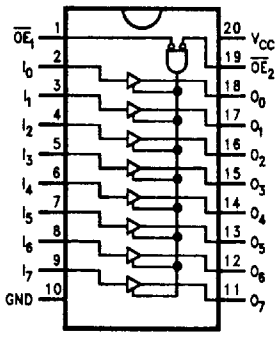
IEE/IEC



TL/F/10989–1

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10989–2

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)
I_n	Inputs
O_n	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
Over Voltage Latchup	V_{CC} +4.5V
DC Latchup Source Current	500 mA
DC Latchup Source Current ($\overline{OE}$)	30 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current		−250		μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{OZ}	Output Leakage Current			±100 ±20	μA		
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			40	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			72	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			7	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	1.7	2.9	5.3	1.7	5.3	ns	8-3
t_{PHL}	Data to Output	2.7	3.9	6.5	2.7	6.5		
t_{PZH}	Output Enable Time	4.4	6.9	12.0	4.4	12.0	ns	8-5
t_{PZL}		3.9	6.0	10.4	3.9	10.4		
t_{PHZ}	Output Disable Time	1.8	3.7	6.2	1.8	6.2	ns	8-5
t_{PLZ}		1.5	3.3	5.4	1.5	5.4		

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 3)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF 1 Output Switching (Note 4)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF 8 Outputs Switching (Notes 3, 4)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	5.0	5.0	6.5	6.0	9.0	ns	8-3
t_{PHL}	Data to Output	4.5	6.5	5.5	7.0	7.0	10.0		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		1.0				1.3	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output		1.2				1.3	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output		3.4				4.0	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output		3.5				4.1	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delay swith 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	13.0	pF	V_{CC} = 5.0V