Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54ALS29825, SN54ALS29826
SN74ALS29825, SN74ALS29826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2829, JANUARY 1986

- **Functionally Equivalent to AMD's AM29825 and AM29826**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effect**
- **Dependable Texas Instruments Quality and Reliability**

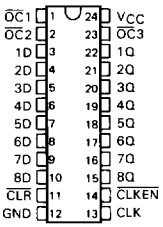
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

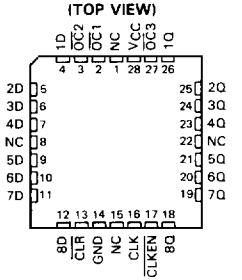
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29825 has non-inverting D inputs and the 'ALS29826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

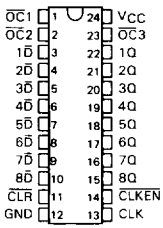
SN54ALS29825 . . . JT PACKAGE
SN74ALS29825 . . . DW OR NT PACKAGE
(TOP VIEW)



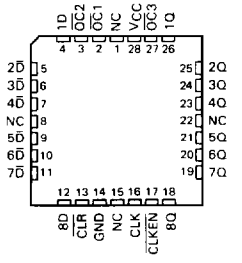
SN54ALS29825 . . . FK PACKAGE
SN74ALS29825 . . . FN PACKAGE
(TOP VIEW)



SN54ALS29826 . . . JT PACKAGE
SN74ALS29826 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS29826 . . . FK PACKAGE
SN74ALS29826 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

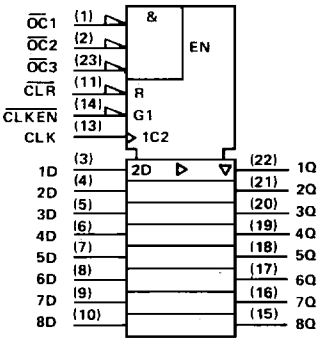
The SN54'family is characterized for operation over the full military temperature range of −55°C to 125°C.
The SN74' family is characterized for operation from 0°C to 70°C.

'ALS29825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

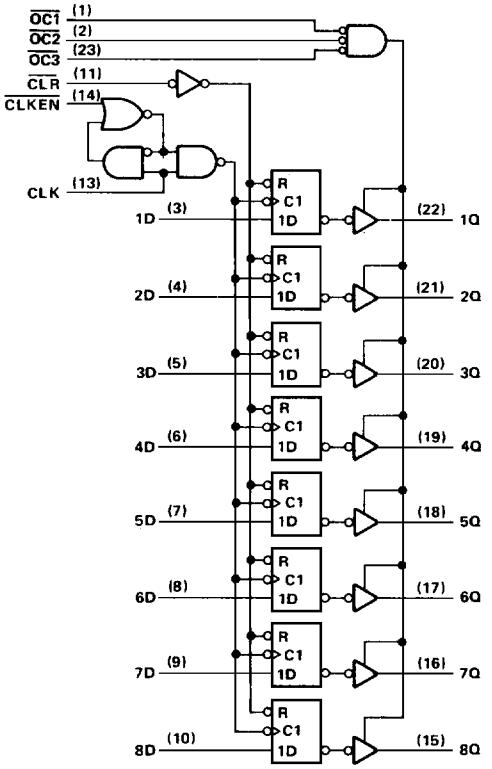
$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 is high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'ALS29825 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for DW, JT, and NT packages.

'ALS29825 logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

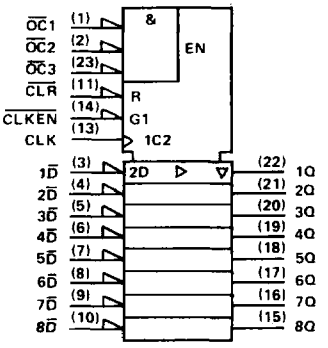
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

'ALS29826 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

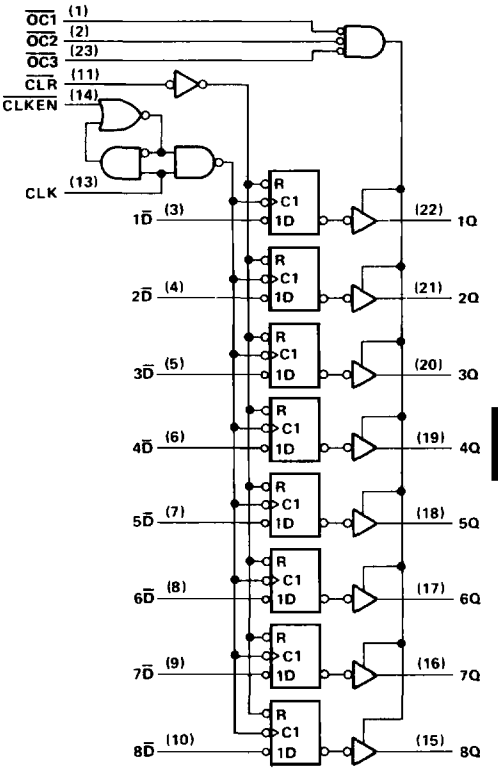
$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 is high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'ALS29826 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, JT, and NT packages.

'ALS29826 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Input current . . . . . 100 mA
Output current . . . . . −30 mA to 5 mA
Operating free-air temperature range:
SN54ALS29825, SN54ALS29826 . . . . . −55°C to 125°C
SN74ALS29825, SN74ALS29826 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65 to 150°C

recommended operating conditions

			SN54ALS29825 SN54ALS29826			SN74ALS29825 SN74ALS29826			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−15			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive							ns
		Data							
		$\overline{CLKEN}$ high or low							
t_h	Hold time, data after CLK↑	Data							ns
		$\overline{CLKEN}$							
T_A	Operating free-air temperature		−55		125	0		70	°C

2 LSI Devices

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54ALS29825 SN54ALS29826			SN74ALS29825 SN74ALS29826			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN to MAX,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = MIN,	I_{OH} = −15 mA	2.4	3.3					
		V_{CC} = MIN,	I_{OH} = −24 mA				2.4	3.2		
V_{OL}		V_{CC} = MIN,	I_{OL} = 32 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = MAX,	V_O = 2.4 V			20			20	μA
I_{OZL}		V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.1			−0.1	mA
I_{OS}§		V_{CC} = MAX,	V_O = 0	−75		−250	−75		−250	mA
I_{CC}	'ALS29825	V_{CC} = MAX	Outputs high							mA
			Outputs low							
			Outputs disabled		48			48		
	'ALS29826		Outputs high							
			Outputs low							
			Outputs disabled		48			48		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = MIN TO MAX,† T_A = MIN TO MAX†				UNIT
				'ALS29825 'ALS29826			SN54ALS29825 SN54ALS29826		SN74ALS29825 SN74ALS29826		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 300 pF								ns
t_{PHL}											
t_{PLH}			C_L = 50 pF		6						
t_{PHL}					7						
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF		13						ns
t_{PZH}	$\overline{OC}$	Any Q	C_L = 300 pF								ns
t_{PZL}											
t_{PZH}			C_L = 50 pF		12						
t_{PZL}					11						
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF								ns
t_{PLZ}											
t_{PHZ}			C_L = 5 pF		5						
t_{PLZ}					6						

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

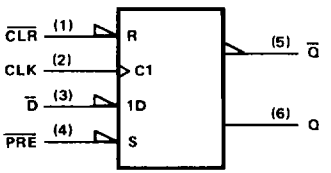
Additional information on these products can be obtained from the factory as it becomes available.

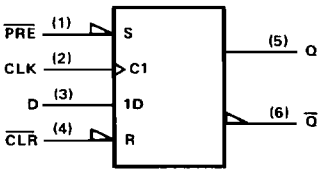
D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

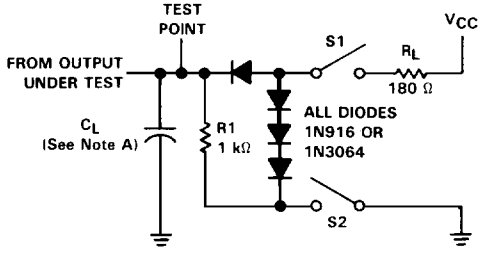
Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pins 5 (Q) is still in phase with the data input D, but now both are considered active high.





2 LSI Devices

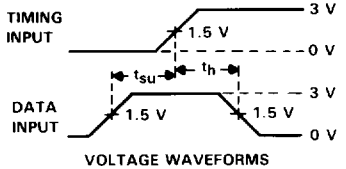
PARAMETER MEASUREMENT INFORMATION



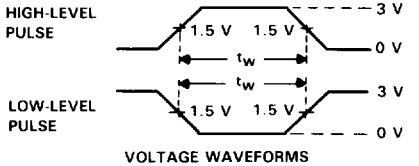
LOAD CIRCUIT

SWITCH POSITION TABLE

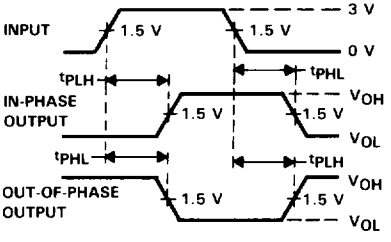
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



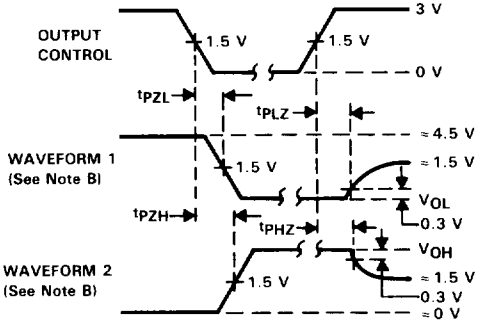
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265