REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add Appendix A for a microcircuit die. Changes in accordance with N.O.R. 5962-R032-97.	96-11-06	R. MONNIN
B	Make changes to boilerplate and add device class T device. - ro	98-12-03	R. MONNIN
C	Add device type 02. - ro	00-08-04	R. MONNIN
D	Make change to propagation delay test for device type 02 as specified under table I. - ro	00-08-29	R. MONNIN
E	Make change to propagation delay test for device type 02 as specified under table I. Updated boilerplate to reflect current requirements. - lgt	01-09-06	R. MONNIN
F	Make correction to DC diode input current description as specified in 1.3. - ro	02-07-09	R. MONNIN
G	Add vendor CAGE F8859. Updated footnote 2/ in table I to accommodate RHA designator "D". - rrp	02-11-27	R. MONNIN
H	Make corrections to title block, figure 1 and figure 2. - ro	05-04-01	R. MONNIN
J	Make change to the output skew test subgroup 10 limit for device type 02 only as specified under Table I. Add paragraphs 2.2 and 6.7. Make changes to paragraph 4.4.4.3 and Table IIB. - ro	09-04-07	J. RODENBECK
K	Add device types 03, 04 and table IB. Make changes to footnote 1/ and add footnote 3/ under Table IIA. Delete Table III and references to device class M requirements. - ro	13-02-27	C. SAFFLE
L	Add case outline Y. Add note under figure 1. - ro	13-06-05	C. SAFFLE
M	Make correction to outline letter E descriptive designator by deleting GDIP2-T16 and replacing with CDIP2-T16 as specified under paragraph 1.2.4. - ro	14-04-15	C. SAFFLE

REV																				
SHEET																				
REV	M	M	M	M	M	M	M	M	M											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	M	M	M	M	M	M	M	M	M	M	M	M	M
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
SANDRA ROONEY

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
95-11-21

MICROCIRCUIT, DIGITAL-LINEAR, RADIATION HARDENED CMOS, QUAD DIFFERENTIAL LINE DRIVER, MONOLITHIC SILICON

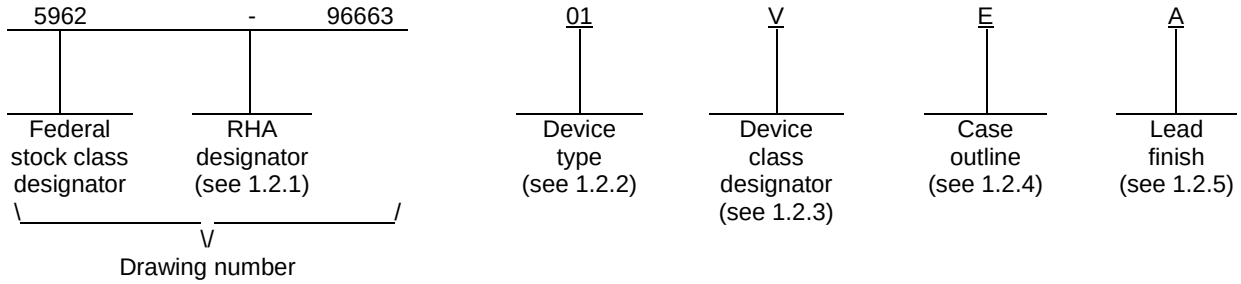
REVISION LEVEL	SIZE	CAGE CODE	
M	A	**67268**	**5962-96663**

SHEET 1 OF 23

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	26C31RH	Radiation hardened quad differential line driver
02	26CLV31RH	Radiation hardened quad differential line driver
03	26C31EH	Radiation hardened quad differential line driver
04	26CLV31EH	Radiation hardened quad differential line driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16	16	Dual-in-line
X	CDFP4-F16	16	Flat pack
Y	CDFP4-F16	16	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 1/

Supply voltage	-0.5 V dc to +7.0 V dc
INPUTS, E, $\overline{E}$ voltage	-0.5 V dc to V_{DD} + 0.5 V dc
Output voltage with power on or off (0 V)	-0.5 V dc to +7.0 V dc
DC diode input current (any input)	$\pm$ 20 mA
DC drain current (any one output)	350 mA
DC V_{DD} or ground current	400 mA
Storage temperature range	-65°C to +150°C
Maximum package dissipation (T_A = +125°C) (P_D): 2/	
Case outline E	0.68 W
Case outlines X and Y	0.44 W
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline E	24°C/W
Case outline X and Y	29°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case outline E	73°C/W
Case outlines X and Y	114°C/W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Operating voltage range:	
Device types 01 and 03	+4.5 V dc to +5.5 V dc
Device types 02 and 04	+3.0 V dc to +3.6 V dc
Input rise and fall time	500 ns maximum
Low input voltage (V_{IL})	0 V to 0.3 V_{DD} maximum
High input voltage (V_{IH})	V_{DD} to +0.7 V_{DD} minimum
Ambient operating temperature (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ If device power exceeds package dissipation capacity, provide heat sinking or derate linearly (the derating is based on (θ_{JA}) at the following rates:

Case outline E	13.7 mW/°C
Case outlines X and Y	8.8 mW/°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):

Device types 01 and 02:

Device classes Q or V ..... 300 krads(Si) 3/

Device class T ..... 100 krads(Si) 3/

Device types 03 and 04 ..... 300 krads(Si) 4/

Maximum total dose available (dose rate ≤ 0.01 rad(Si)/s):

Device types 03 and 04 ..... 50 krads(Si) 4/

Single event phenomena (SEP):

No SEL occurs at effective LET (see 4.4.4.2.2) ..... ≤ 100 MeV/mg/cm^2 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3/ Device types 01 and 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si) for device class V or Q and 100 krads(Si) for device class T.

4/ Device types 03 and 04 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si), and condition D to a maximum total dose of 50 krads(Si).

5/ Limits obtained during technology characterization/qualification, guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = 4.5 V and 5.5 V 3/ 4/ I_O = -20 mA	1,2,3	01,03	2.5		V
		V_{DD} = 3.0 V and 3.6 V 3/ 4/ I_O = -20 mA		02,04	1.8		
Low level output voltage	V_{OL}	V_{DD} = 4.5 V and 5.5 V 3/ 4/ I_O = 20 mA	1,2,3	01,03		0.5	V
		V_{DD} = 3.0 V and 3.6 V 3/ 4/ I_O = 20 mA		02,04		0.5	
Differential output voltage	V_T, $\overline{VT}$	$V_{DD} = V_{IH}$ = 4.5 V, 5/ $R_L = R_1 + R_2$, V_{IL} = 0 V	1,2,3	01,03	2.0		V
		$V_{DD} = V_{IH}$ = 3.0 V, 5/ $R_L = R_1 + R_2$, V_{IL} = 0 V		02,04	1.8		
Difference in differential output	$\lvert V_T \rvert - \lvert \overline{VT} \rvert$	$V_{DD} = V_{IH}$ = 4.5 V, 5/ $R_L = R_1 + R_2$, V_{IL} = 0 V	1,2,3	01,03		0.4	V
		$V_{DD} = V_{IH}$ = 3.0 V, 5/ $R_L = R_1 + R_2$, V_{IL} = 0 V		02,04		0.4	
Common mode output voltage	V_{OS}, $\overline{VOS}$	$V_{DD} = V_{IH}$ = 4.5 V, 5/ $R_L = R_1 + R_2$, V_{IL} = 0 V	1,2,3	01,03		3.0	V
		$V_{DD} = V_{IH}$ = 3.0 V, 5/ $R_L = R_1 + R_2$, V_{IL} = 0 V		02,04		3.0	
Difference in common mode output voltage	$\lvert V_{OS} \rvert - \lvert \overline{VOS} \rvert$	$V_{DD} = V_{IH}$ = 4.5 V, 5/ $R_L = R_1 + R_2$, V_{IL} = 0 V	1,2,3	01,03		0.4	V
		$V_{DD} = V_{IH}$ = 3.0 V, 5/ $R_L = R_1 + R_2$, V_{IL} = 0 V		02,04		0.4	
High level input voltage	V_{IH}	V_{DD} = 4.5 V, 5.5 V 6/	1,2,3	01,03	$0.7V_{DD}$		V
		V_{DD} = 3.0 V, 3.6 V 6/		02,04	$0.7V_{DD}$		
Low level input voltage	V_{IL}	V_{DD} = 4.5 V, 5.5 V 6/	1,2,3	01,03		$0.3V_{DD}$	V
		V_{DD} = 3.0 V, 3.6 V 6/		02,04		$0.3V_{DD}$	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Standby supply current	I_{DDSB}	V_{DD} = 5.5 V, Output = OPEN, $V_{IN} = V_{DD}$ or GND	1,2,3	01,03		500	µA
		V_{DD} = 3.6 V, Output = OPEN, $V_{IN} = V_{DD}$ or GND		02,04		100	
Three-state output leakage current	I_{OZ}	V_{DD} = 5.5 V, 7/ force voltage = 0 V or V_{CC}	1,2,3	01,03		±5	µA
		V_{DD} = 3.6 V, 7/ force voltage = 0 V or V_{CC}		02,04		±5	
Input leakage	I_{IN}	V_{DD} = 5.5 V, $V_{IN} = V_{DD}$ or GND	1,2,3	01,03		±1.0	µA
		V_{DD} = 3.6 V, $V_{IN} = V_{DD}$ or GND		02,04		±1.0	
Output leakage current power OFF	I_{OFF}	V_{DD} = 0 V, V_{OUT} = 6 V, -250 mV inputs = GND	1,2,3	01,02, 03,04	-100	+100	µA
Input clamp voltage	V_{IC}	At -1.0 mA	1,2,3	01,02,		-1.5	V
		At +1.0 mA		03,04		+1.5	
Input capacitance	C_{IN}	V_{DD} = open, 8/ 9/ f = 1 MHz	4	01,02, 03,04		12	pF
Output capacitance	C_{OUT}	V_{DD} = open, 8/ 9/ f = 1 MHz	4	01,02, 03,04		12	pF
Operating short circuit	I_{OS}	V_{DD} = 5.5 V, 8/ 9/ 10/ $V_{IN} = V_{DD}$ or GND, V_{OUT} = 0 V	1,2,3	01,03	-30	-150	mA
		V_{DD} = 3.6 V, 8/ 9/ 10/ $V_{IN} = V_{DD}$ or GND, V_{OUT} = 0 V		02,04	-30	-150	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
On-state resistance	R_{ON}	V_{DD} = 4.5 V, 8/ 9/ V_{OUT} = 1.5 V, V_{IN} = V_{DD} or GND	4,5,6	01,03		10	Ω
		V_{DD} = 3.0 V, 8/ 9/ V_{OUT} = 1.5 V, V_{IN} = V_{DD} or GND		02,04		10	
Propagation delay	t_{PLH}, t_{PHL}	V_{DD} = 4.5 V 11/	9,10,11	01,03	2	22	ns
	t_{PZH}, t_{PZL}	V_{DD} = 4.5 V 11/			5	28	
	t_{PHZ}, t_{PLZ}	V_{DD} = 4.5 V 11/			2	22	
Propagation delay	t_{PLH}, t_{PHL}	V_{DD} = 3.0 V 11/	9,10,11	02,04	2	30	ns
	t_{PZH}, t_{PZL}	V_{DD} = 3.0 V 11/			5	42	
	t_{PHZ}, t_{PLZ}	V_{DD} = 3.0 V 11/			2	28	
Output skew	t_{SKEW}	V_{DD} = 4.5 V, 11/ 12/ R_L = 100 Ω, C_L = 40 pF	9,10,11	01,03		3	ns
		V_{DD} = 3.0 V, 11/ 12/	9,11	02,04		5	
		R_L = 100 Ω, C_L = 40 pF	10			7	
Rise and fall times	t_{THL}, t_{TLH}	V_{DD} = 4.5 V 11/	9,10,11	01,03	1	10	ns
		V_{DD} = 3.0 V 11/		02,04	1	14	

1/ All voltages referenced to device ground.

2/ RHA device types 01 and 02 (device classes Q and V) supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation, and device type 01 (device class T) will meet all levels M, D, P, L and R of irradiation. However, device types 01 and 02 (device classes Q and V) are only tested at the "D" or "F" levels depending on the manufacturer, and device type 01 (device class T) is only tested at the "R" level in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein).

RHA device types 03 and 04 supplied to this drawing will meet all levels M, D, P, L, R, and F of irradiation for condition A and M, D, P, and L for condition D. However, device type 04 is only tested at the "F" level in accordance with MIL-STD-883, method 1019, condition A and tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).

Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ Force / measure functions may be interchanged.

4/ V_{IL} = 0.3 V_{DD}, V_{IH} = 0.7 V_{DD}.

5/ These test conditions are detailed in EIA specification RS-422. R_1 = R_2 = 50 Ω.

6/ This parameter tested as inputs levels in V_{OL} / V_{OH}, I_{OZ}, functional test and/or discrete voltage level.

TABLE IA. Electrical performance characteristics - Continued.

7/ The input is conditioned to have the output in the opposite state of the forcing I_{OZ} condition.
8/ These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major design or process changes that affect these parameters.
9/ Post irradiation electrical performance testing not performed for these parameters.
10/ Only one output at a time may be shorted.
11/ See table EIA RS-422. See figure 3.
12/ Skew is defined as the difference in propagation delays between complementary outputs at the 50 % point.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP	Bias V_{DD}	Effective linear energy transfer (LET)
01, 02	No SEL	5.5 V	LET $\leq$ 100 MeV/mg/cm^2
03, 04	No SEL	3.6 V	LET $\leq$ 100 MeV/mg/cm^2

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by technical review board and qualifying activity.
3/ Tested for single event latch up at worse case temperature, T_A = +125°C $\pm$ 10°C.

Case outlines	E, X, and Y SEE NOTE
Device types	01, 02, 03, and 04
Terminal number	Terminal symbol
1	A_{IN}
2	A_O
3	$\overline{A}_O$
4	ENABLE
5	$\overline{B}_O$
6	B_O
7	B_{IN}
8	GND
9	C_{IN}
10	C_O
11	$\overline{C}_O$
12	$\overline{ENABLE}$
13	$\overline{D}_O$
14	D_O
15	D_{IN}
16	V_{DD}

Note: For case outline Y only, the lid is grounded.

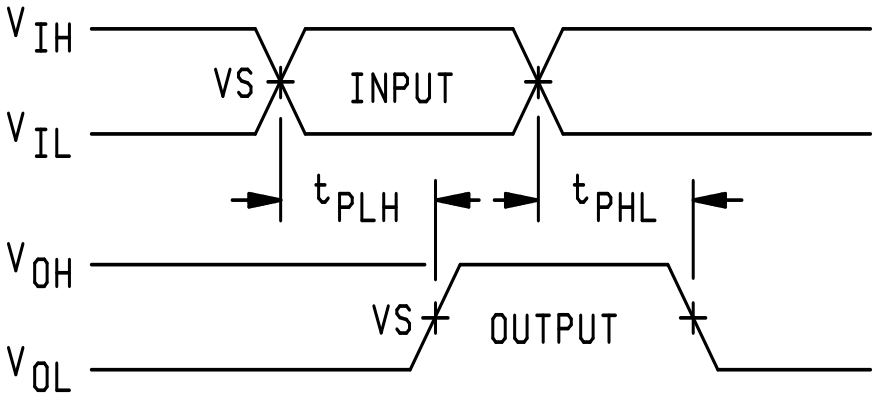
FIGURE 1. Terminal connections.

DEVICE POWER	INPUTS			OUTPUTS	
ON / OFF	ENABLE	$\overline{ENABLE}$	IN	OUT	$\overline{OUT}$
ON	0	1	X	HI-Z	HI-Z
ON	1	X	0	0	1
ON	X	0	0	0	1
ON	1	X	1	1	0
ON	X	0	1	1	0
OFF(0 V)	X	X	X	HI-Z	HI-Z

X = Don't care
0 = Low
1 = High

FIGURE 2. Truth table.

Propagation delay timing diagram



NOTE: Voltage levels

V_{DD} = 4.50 V for device types 01, 03 and V_{DD} = 3.0 V for device types 02, 04.

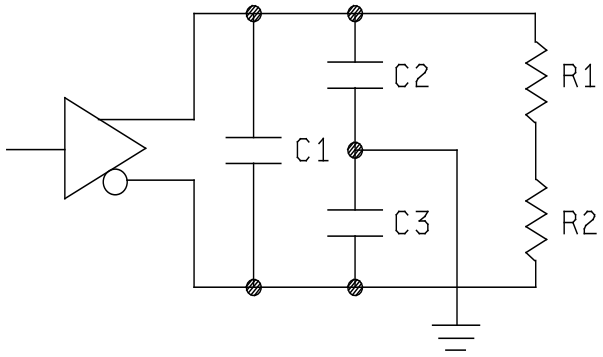
V_{IH} = 4.50 V for device types 01, 03 and V_{IH} = 3.0 V for device types 02, 04.

V_S = 50 %

V_{IL} = 0 V

GND = 0 V

Propagation delay load circuit

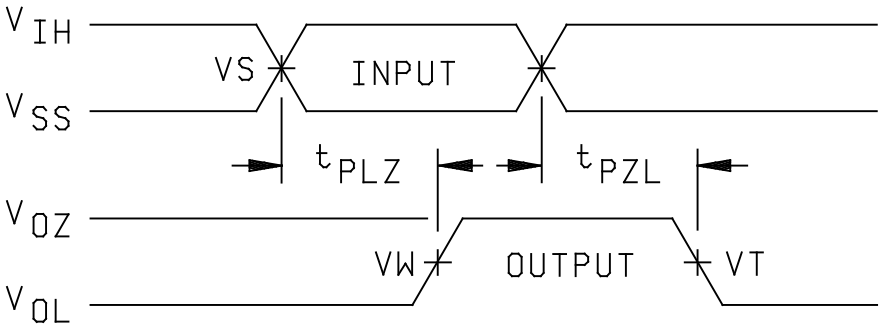


C1 = C2 = C3 = 40 pF

R1 = R2 = 50 Ω

FIGURE 3. Timing and load circuit diagrams.

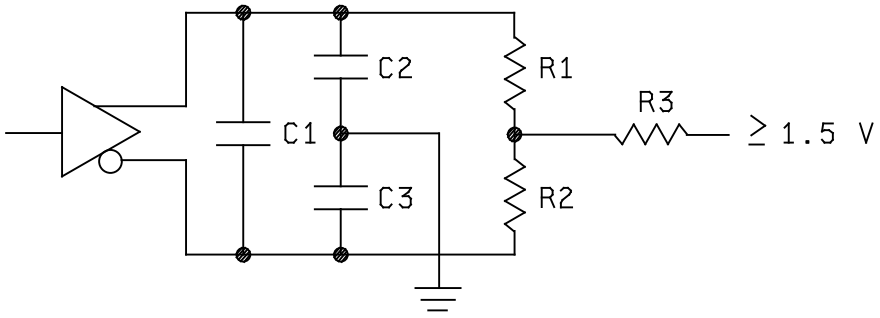
Three-state low timing diagram



NOTE: Voltage levels

V_{DD} = 4.50 V for device types 01, 03 and V_{DD} = 3.0 V for device types 02, 04.
V_{IH} = 4.50 V for device types 01, 03 and V_{IH} = 3.0 V for device types 02, 04.
V_S = 50 %
$V_W = V_{OL}$ + 0.3 V
V_T = 0.80 V

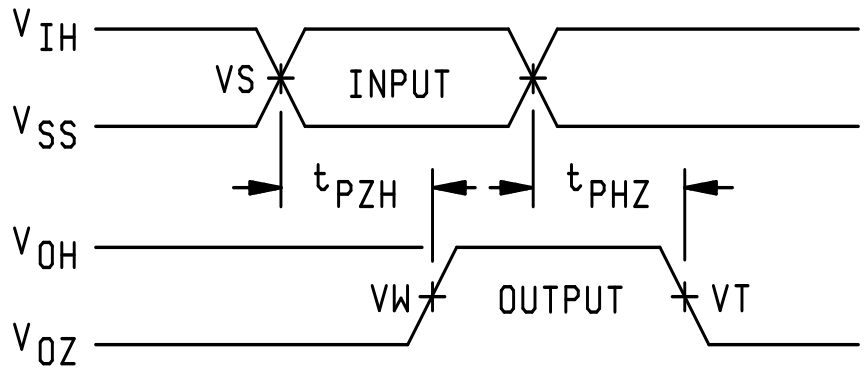
Three-state low load circuit



C1 = C2 = C3 = 40 pF
R1 = R2 = 50 Ω
R3 = 500 Ω

FIGURE 3. Timing and load circuit diagrams - Continued.

Three-state high timing diagram



NOTE: Voltage levels

V_{DD} = 4.50 V for device types 01, 03 and V_{DD} = 3.0 V for device types 02, 04.

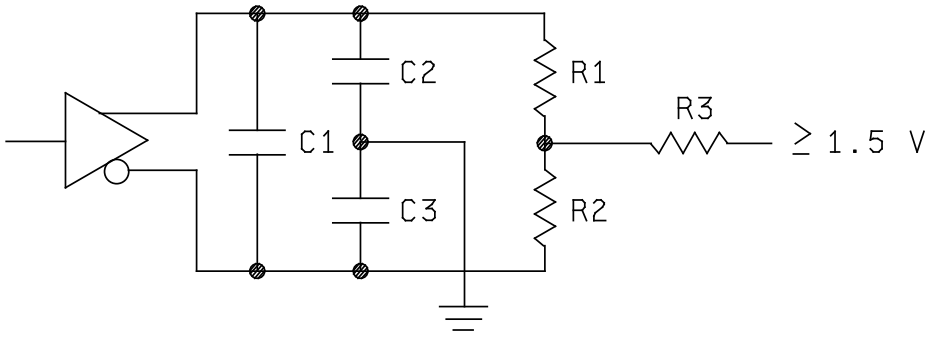
V_{IH} = 4.50 V for device types 01, 03 and V_{IH} = 3.0 V for device types 02, 04.

V_S = 50 %

$V_W = V_{OL} + 0.3$ V

V_T = 2.00 V

Three-state high load circuit



C1 = C2 = C3 = 40 pF

R1 = R2 = 50 Ω

R3 = 500 Ω

FIGURE 3. Timing and load circuit diagrams - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) should be measured for initial qualification and after any process or design changes which may affect input or output capacitance.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,7,8, 1/ 9,10,11	1,2,3, 1/ 2/ 7,8,9,10,11,Δ	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,4,5, 3/ 6,7,8,9,10,11	1,2,3,4,5, 3/ 6,7,8,9,10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8, 9,10,11	1,2,3,7,8, 2/ 9,10,11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	As specified in QM plan

1/ PDA applies to subgroup 1. For class V to subgroups 1, 7, 9, and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).
3/ Subgroups 4, 5, and 6, if not tested, shall be guaranteed to the limits specified in table IA.

TABLE IIB. Burn-in delta parameters and group C delta parameters at (+25°C). 1/

Parameters	Symbol	Delta limits
Standby supply current	I_{DDSB}	±100 μA
Three state output leakage current	I_{OZ}	±1.0 μA
Low level output voltage	V_{OL}	±60 mV
High level output voltage	V_{OH}	±150 mV
Input leakage current	I_{IL}, I_{IH}	±150 nA

1/ If device is tested at or below limits in table, no deltas are required. Deltas are performed at room temperature.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, 03, and 04. In addition, for device types 03 and 04 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

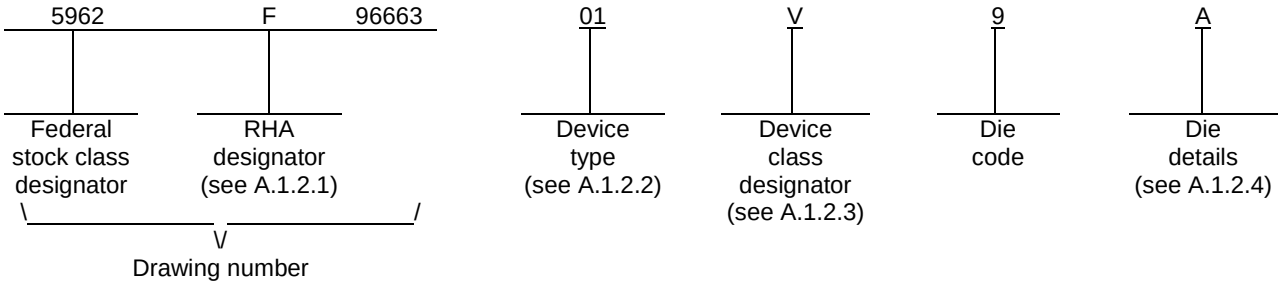
b. Number of latch ups (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96663

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	26C31RH	Radiation hardened quad differential line driver
02	26CLV31RH	Radiation hardened quad differential line driver
03	26C31EH	Radiation hardened quad differential line driver
04	26CLV31EH	Radiation hardened quad differential line driver

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03, 04	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.2.1, and 4.4.4.2.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

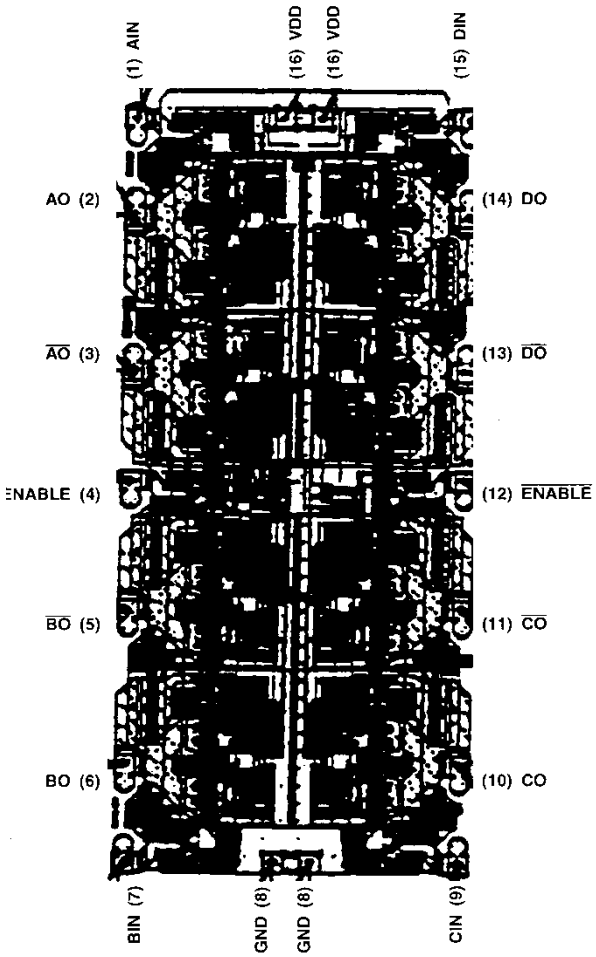
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines E, X, and Y (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die bonding pad locations and electrical functions.

Die physical dimensions.
Die size: 2450 microns x 4950 microns.
Die thickness: 21 ± 1 mils.

Interface materials.
Top metallization: Si Al Cu 10.0 kÅ ± 2 kÅ
Backside metallization: None: chemical etch

Glassivation.
Type: PSG
Thickness: 8 kÅ ± 1 kÅ

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: Substrate internally tied to V_{DD}.
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-04-15

Approved sources of supply for SMD 5962-96663 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962D9666301QEA	3/	RHD26C31D09Q
5962D9666301QEC	3/	RHD26C31D08Q
5962D9666301QXA	3/	RHD26C31K02Q
5962D9666301QXC	3/	RHD26C31K01Q
5962F9666301QEC	34371	HS1-26C31RH-8
5962F9666301QXC	34371	HS9-26C31RH-8
5962D9666301VEA	3/	RHD26C31D09V
5962D9666301VEC	3/	RHD26C31D08V
5962D9666301VXA	3/	RHD26C31K02V
5962D9666301VXC	3/	RHD26C31K01V
5962F9666301VEC	34371	HS1-26C31RH-Q
5962F9666301VXC	34371	HS9-26C31RH-Q
5962F9666301VYC	34371	HS9G-26C31RH-Q
5962F9666301V9A	34371	HS0-26C31RH-Q
5962R9666301TEC	34371	HS1-26C31RH-T
5962R9666301TXC	34371	HS9-26C31RH-T
5962F9666302QEC	34371	HS1-26CLV31RH-8
5962F9666302QXC	34371	HS9-26CLV31RH-8
5962F9666302VEC	34371	HS1-26CLV31RH-Q
5962F9666302VXC	34371	HS9-26CLV31RH-Q
5962F9666302VYC	34371	HS9G-26CLV31RH-Q
5962F9666302V9A	34371	HS0-26CLV31RH-Q
5962R9666302TEC	34371	HS1-26CLV31RH-T
5962R9666302TXC	34371	HS9-26CLV31RH-T

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9666303VEC	34371	HS1-26C31EH-Q
5962F9666303VXC	34371	HS9-26C31EH-Q
5962F9666303V9A	34371	HS0-26C31EH-Q
5962F9666304VEC	34371	HS1-26CLV31EH-Q
5962F9666304VXC	34371	HS9-26CLV31EH-Q
5962F9666304VYC	34371	HS9G-26CLV31EH-Q
5962F9666304V9A	34371	HS0-26CLV31EH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803