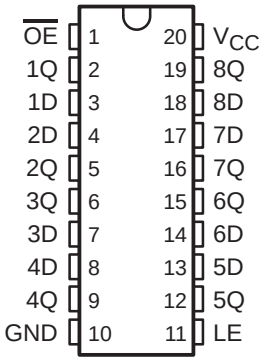
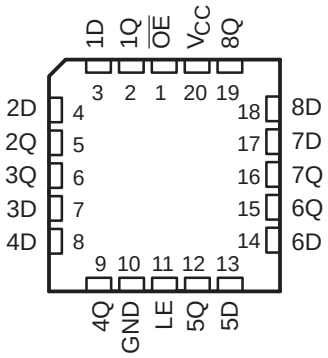
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV373 . . . J OR W PACKAGE
SN74LV373 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV373 . . . FK PACKAGE
(TOP VIEW)



description

These octal transparent D-type latches are designed for 2.7-V to 5.5-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

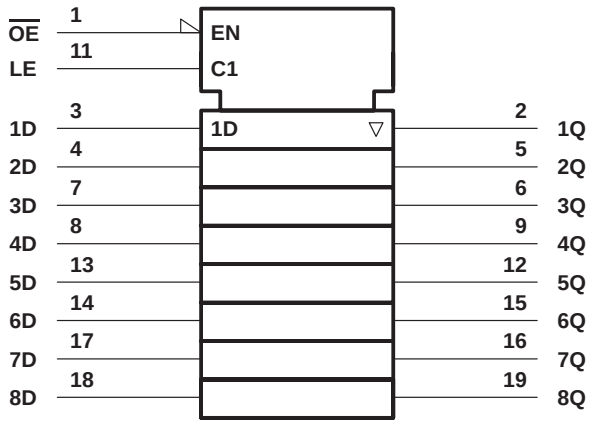
The SN74LV373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

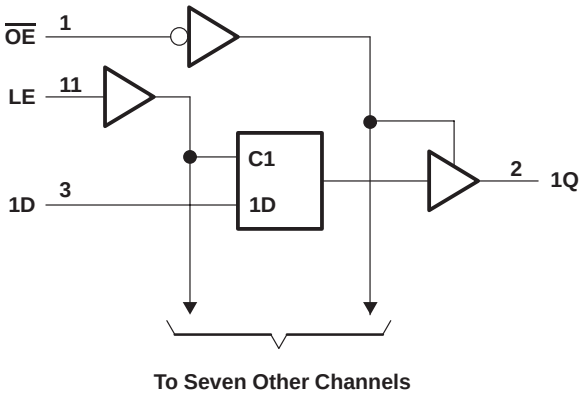
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DB, DW, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package . . . . . 0.6 W
DW package . . . . . 1.6 W
PW package . . . . . 0.7 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV373		SN74LV373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–8		–8	mA
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV373			SN74LV373			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA	MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –8 mA	3 V	2.4			2.4			
	I_{OH} = –16 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
	I_{OL} = 8 mA	3 V			0.4			0.4	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±5			±5	μA
		5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		
C_o	V_O = V_{CC} or GND	3.3 V		7			7		pF
		5 V		7.5			7.5		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV373						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		10		10		8		ns
t_{su}	Setup time, data before LE↓	High or low	4		6		6		ns
t_h	Hold time, data after LE↓	High or low	6		6		6		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV373						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		10		10		8		ns
t_{su}	Setup time, data before LE↓	High or low	4		6		6		ns
t_h	Hold time, data after LE↓	High or low	6		6		6		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV373								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q		8	16		11	22		28	ns
	LE			11	19		15	25		26	
t_{en}	$\overline{OE}$	Q		15	23		15	27		28	ns
t_{dis}	$\overline{OE}$	Q		15	23		15	27		28	ns

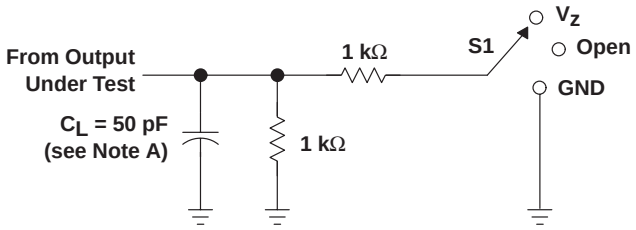
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV373								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q		8	16		11	22		28	ns
	LE			11	19		15	25		26	
t_{en}	$\overline{OE}$	Q		15	23		15	27		28	ns
t_{dis}	$\overline{OE}$	Q		15	23		15	27		28	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	47	pF
		Outputs disabled			29	
		Outputs enabled		5 V	112	
		Outputs disabled			62	

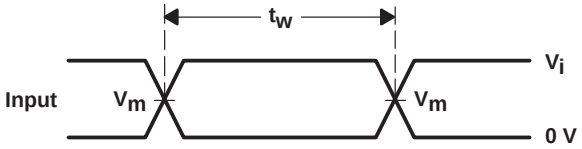
PARAMETER MEASUREMENT INFORMATION



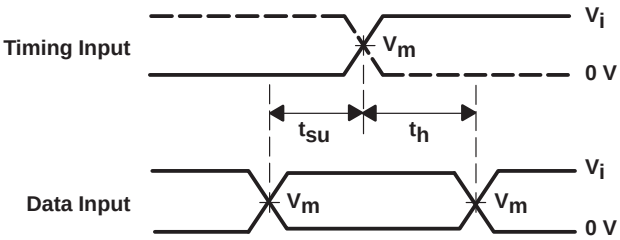
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

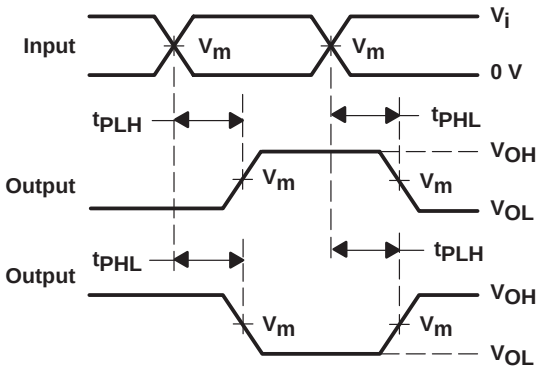
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	$0.5 \times V_{CC}$	1.5 V
V_i	V_{CC}	2.7 V
V_z	$2 \times V_{CC}$	6 V



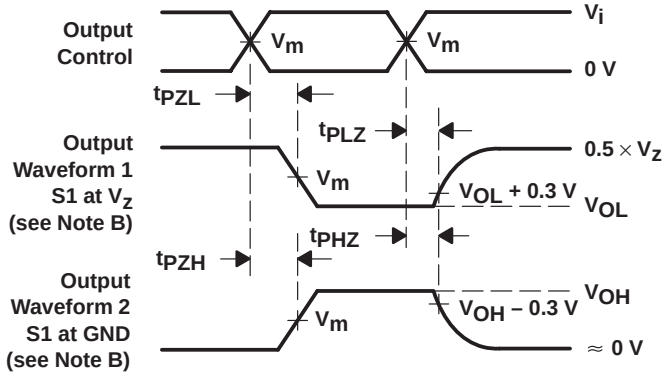
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LV373DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74LV373DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74LV373DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74LV373PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265