



# HIGH-SPEED CMOS 8-INPUT MULTIPLEXER

IDT74FCT251AT/CT

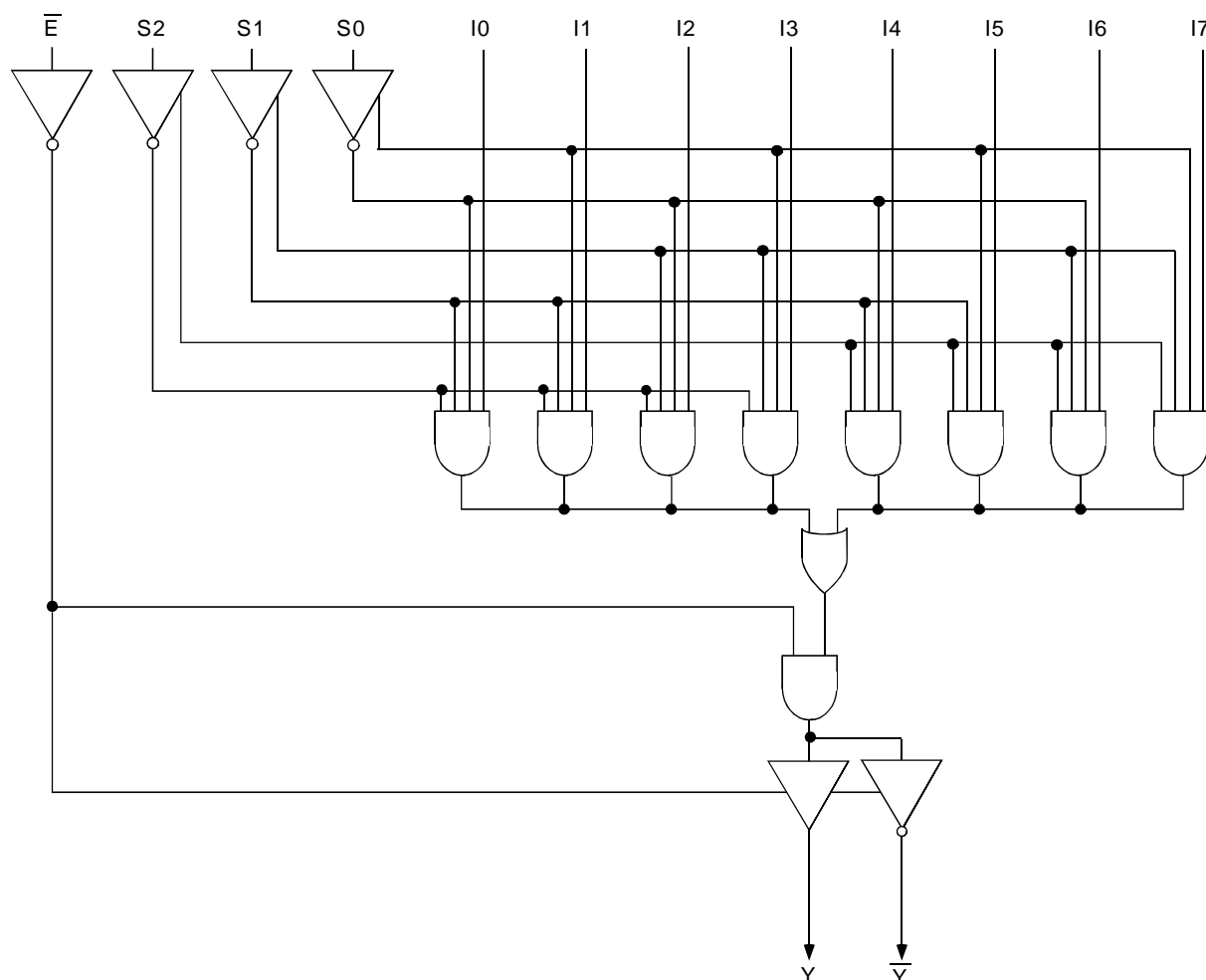
## FEATURES:

- Pin and function compatible to the Quality QS74FCT family
- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- JEDEC FCT spec. compatible
- A and C speed grades with 4.5ns tPD for C
- IOL = 48mA
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

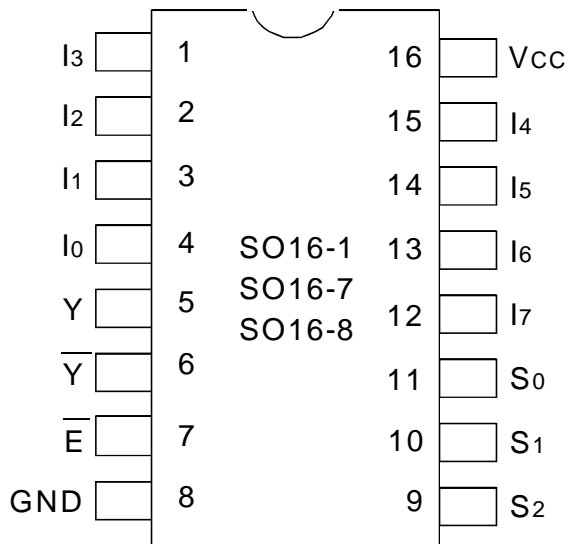
## DESCRIPTION:

The IDT74FCT251T is a high-speed CMOS TTL-compatible 8-input multiplexer with 3-state outputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SOIC/ QSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Max.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

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### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
I <sub>x</sub>	I	Data In
S <sub>x</sub>	I	Select
$\bar{E}$	I	Enable
Y, $\bar{Y}$	O	Data Out

## FUNCTION TABLE (1)

$\bar{E}$	Select			Outputs		Function
	S2	S1	S0	Y	$\bar{Y}$	
H	X	X	X	Hi-Z	Hi-Z	Disable
L	L	L	L	I <sub>0</sub>	$\bar{I}_0$	S2-0 = 0
L	L	L	H	I <sub>1</sub>	$\bar{I}_1$	S2-0 = 1
L	L	H	L	I <sub>2</sub>	$\bar{I}_2$	S2-0 = 2
L	L	H	H	I <sub>3</sub>	$\bar{I}_3$	S2-0 = 3
L	H	L	L	I <sub>4</sub>	$\bar{I}_4$	S2-0 = 4
L	H	L	H	I <sub>5</sub>	$\bar{I}_5$	S2-0 = 5
L	H	H	L	I <sub>6</sub>	$\bar{I}_6$	S2-0 = 6
L	H	H	H	I <sub>7</sub>	$\bar{I}_7$	S2-0 = 7

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs		—	0.2	—	V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} < V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current						
$I_{OZ}$	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$		-60	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^\circ\text{C}^{(3)}$		—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 48\text{mA}$	—	—	0.5	V

### NOTES:

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
3. This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$I_{CCD}$	Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ freq = 0	—	2	mA
$I_C$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/ MHz

### NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ). All other inputs at  $V_{CC}$  or GND.
3. For flip-flops,  $I_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4\text{V}$ )  
 $DH$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $DH$   
 $I_{CCD}$  = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_i$  = Input Frequency  
 $N_i$  = Number of Inputs at  $f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE(1)**

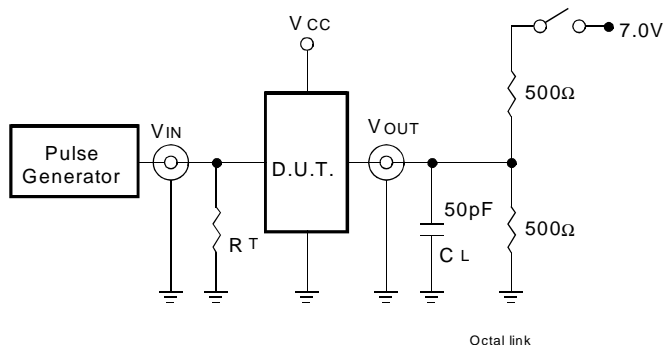
Symbol	Parameter <sup>(2)</sup>	74FCT251AT		74FCT251CT		Unit
		Min.	Max.	Min.	Max.	
t <sub>IV</sub>	Propagation Delay I <sub>n</sub> to Y or $\bar{Y}$	1.5	5.2	1.5	4.5	ns
t <sub>SY</sub>	Propagation Delay S <sub>n</sub> to Y or $\bar{Y}$	1.5	6.6	1.5	5.9	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\bar{E}$ to Y <sub>i</sub>	1.5	6	1.5	5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Enable Time $\bar{E}$ to Y <sub>i</sub>	1.5	6	1.5	5	ns

**NOTES:**

1. C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

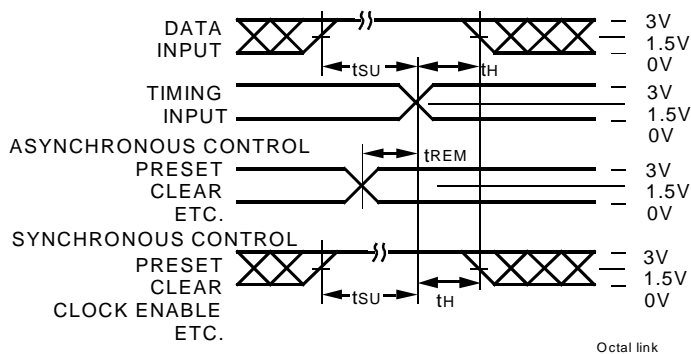
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

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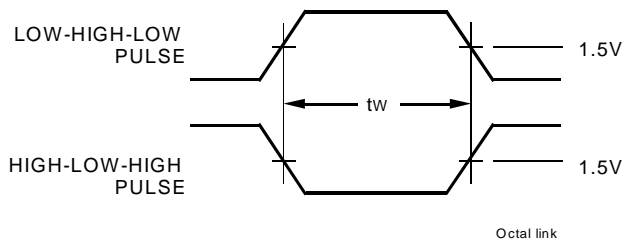
#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

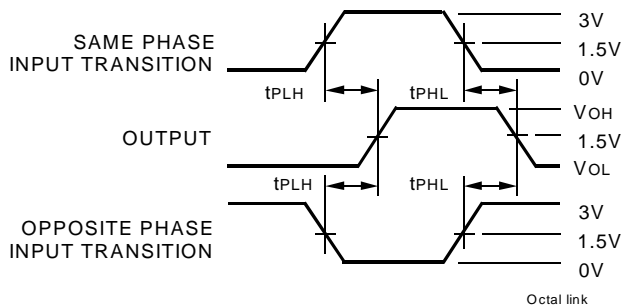
### SET-UP, HOLD, AND RELEASE TIMES



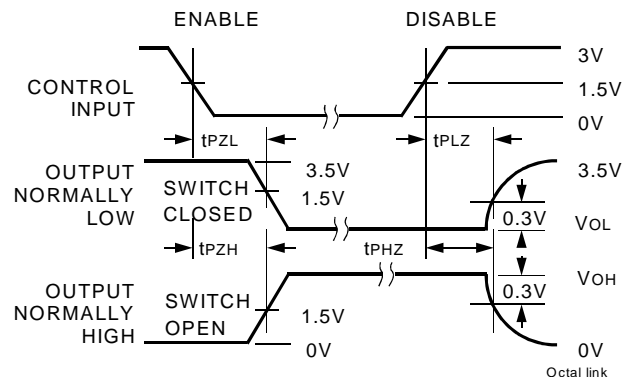
### PULSE WIDTH



### PROPAGATION DELAY



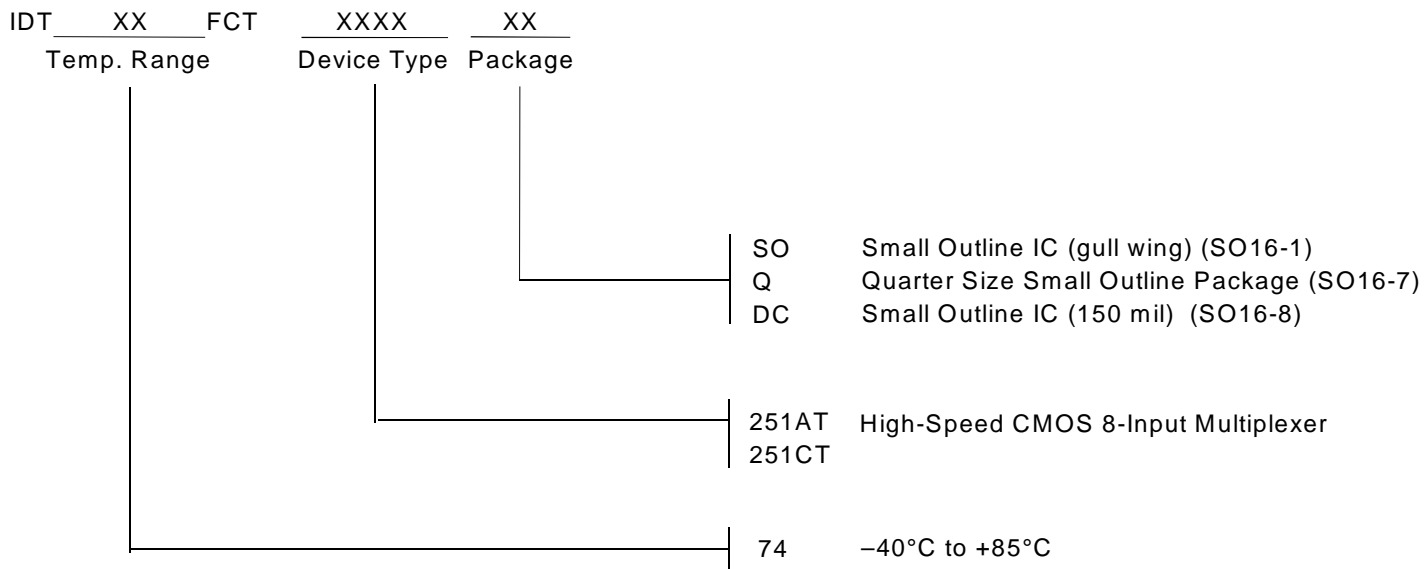
### ENABLE AND DISABLE TIMES



#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_F \leq 2.5\text{ns}$ ;  $t_R \leq 2.5\text{ns}$

### ORDERING INFORMATION



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