High Speed CMOS 8-Bit Buffers/Line Drivers

QS54/74FCT540T
QS54/74FCT541T

QS54/74FCT2540T
QS54/74FCT2541T

FEATURES/BENEFITS

- Pin and function compatible to the 74F540/1 74FCT540/1 and 74FCT540T/1T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T540T/1T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std. thru D speed grades with 3.8ns tPD for D
- Iol = 64 mA Com., 48mA Mil.

FCT-T 2540T/1T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. thru D speed grades with 3.8ns tPD for D
- Iol = 12mA Com.

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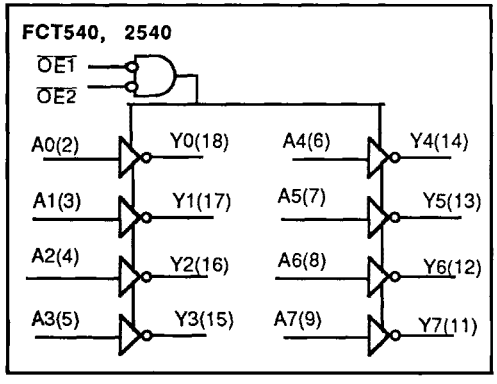
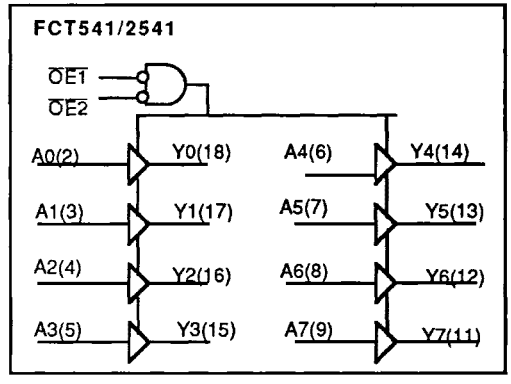
DESCRIPTION

The QSFCT540T and QSFCT541T are 8-bit buffers/line drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. The FCT2540 and FCT2541 are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2540 series parts can replace the 540 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

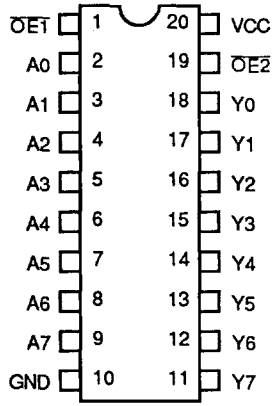




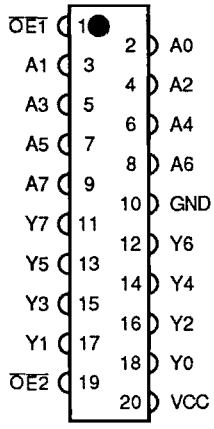
PINOUTS

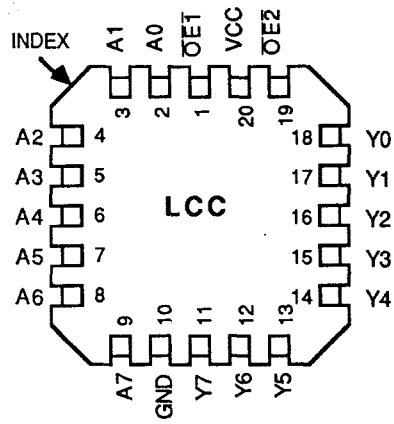
FCT540/541
FCT2540/2541

PDIP, SOIC, QSOP



ZIP





ALL PINS TOP VIEW

FUNCTION TABLES

FCT540/2540, FCT541/2541

$\overline{OE1}$	$\overline{OE2}$	Input A	540	541	Function
			Output Y	Output Y	
H	X	X	Hi-Z	Hi-Z	Disable Outputs
X	H	X	Hi-Z	Hi-Z	
L	L	L	H	L	Enable Outputs
L	L	H	L	H	

H=High, L=Low, Z=High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to 7.0V
DC Input Voltage V_I ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0..... -20 mA
DC Output Diode Current with V_O <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
Maximum Power Dissipation..... 0.5 watts
T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,19	4	4	5	7	pF
———	6	6	7	9	pF
2-9,11-18	8	8	9	10	pF

Note: Capacitance is characterized but not tested

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysterisis	Vtlh - Vthl for All Inputs		-	0.2	-	
| Iih | | Iil |	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	µA
| Ioz |	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-225	mA
Ior	Current Drive FCT2XXX (25Ω)	Vcc = Min, Vo =2.0V (3)		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 48 mA (MIL)	-	-	0.55	
			Iol = 64 mA (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	25	-	Ω
			Iol = 12 mA (COM)	20	28	40	

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, freq = 0 0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc	-	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = MAX, Vin =3.4 V, freq = 0 (2)	-	2.0	
Qccd	Supply Current per input per mHz	Vcc = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

540 / 2540 (3)

Symbol	Parameter		540T, 2540T		540AT, 2540AT		540CT, 2540CT		540DT, 2540DT		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH, tPHL	Propagation Delay Ai to Yi (1)	Com	1.5	8.5	1.5	4.8	1.5	4.1	1.5	3.8	ns
tPLH, tPHL	Propagation Delay Ai to Yi (1)	Mil	1.5	9.5	1.5	5.1	1.5	4.6	1.5	4.4	
tPZH, tPZL	Output Enable Time $\overline{OE}$ toYi (1)	Com	1.5	10	1.5	6.2	1.5	5.8	1.5	5.2	
tPZH, tPZL	Output Enable Time $\overline{OE}$ toYi (1)	Mil	1.5	10.5	1.5	6.5	1.5	6.5	1.5	6.5	
tPLZ, tPHZ	Disable Time (1)	Com	1.5	9.5	1.5	5.6	1.5	5.2	1.5	5.2	
tPLZ, tPHZ	Disable Time (1)	Mil	1.5	12.5	1.5	5.9	1.5	5.7	1.5	5.7	

Notes:
1. Minimum propagation delay values are guaranteed but not tested.
2. This parameter is guaranteed but not tested.

541 / 2541(3)

Symbol	Parameter		541T, 2541T		541AT, 2541AT		541CT, 2541CT		541DT, 2541DT		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH, tPHL	Propagation Delay Ai to Yi (1)	Com	1.5	8	1.5	4.8	1.5	4.1	1.5	3.8	ns
tPLH, tPHL	Propagation Delay Ai to Yi (1)	Mil	1.5	9	1.5	5.1	1.5	4.6	1.5	4.4	
tPZH, tPZL	Output Enable Time $\overline{OE}$ toYi (1)	Com	1.5	10	1.5	6.2	1.5	5.8	1.5	5.2	
tPZH, tPZL	Output Enable Time $\overline{OE}$ toYi (1)	Mil	1.5	10.5	1.5	6.5	1.5	6.5	1.5	6.5	
tPLZ, tPHZ	Disable Time (1)	Com	1.5	9.5	1.5	5.6	1.5	5.2	1.5	5.2	
tPLZ, tPHZ	Disable Time (1)	Mil	1.5	12.5	1.5	5.9	1.5	5.7	1.5	5.7	

Notes:
1) Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) See Test Circuit and Waveforms.