



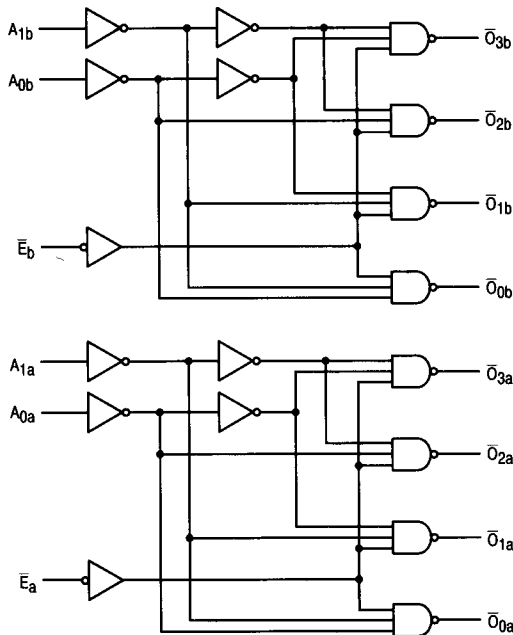
Dual 2-of-4 Line Decoder

**ELECTRICALLY TESTED PER:
MIL-M-38510/30702**

The LSTTL/MSI 54LS139 is a high-speed 1-of-4 Decoder/Demultiplexer. This device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active Low Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'LS139 can be used as a function generator providing all four minterms of two variables. The 'LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Demultiplexing Capability
- Multiple Input Enable For Easy Expansion
- Typical Power Dissipation of 32 mW
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High-Speed Termination Effect

LOGIC DIAGRAM



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Military 54LS139



AVAILABLE AS:

- 1) JAN: JM38510/30702BXA
- 2) SMD: 7600501
- 3) 883: 54LS139/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2**

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
E _a	1	1	2	VCC
A _{0a}	2	2	3	VCC
A _{1a}	3	3	4	VCC
O _{0a}	4	4	5	VCC
O _{1a}	5	5	7	VCC
O _{2a}	6	6	8	VCC
O _{3a}	7	7	9	VCC
GND	8	8	10	GND
O _{3b}	9	9	12	VCC
O _{2b}	10	10	13	VCC
O _{1b}	11	11	14	VCC
O _{0b}	12	12	15	VCC
A _{1b}	13	13	17	VCC
A _{0b}	14	14	18	VCC
E _b	15	15	19	VCC
VCC	16	16	20	VCC

**BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX**

TRUTH TABLE

Inputs			Outputs			
E	A ₀	A ₁	O ₀	O ₁	O ₂	O ₃
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Don't Care

FUNCTIONAL DESCRIPTION

The 'LS139 is a high-speed dual 1-of-4 Decoder/ Demultiplexer fabricated with the low power Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\bar{O}_0-\bar{O}_3$). Each decoder has an active LOW Enable (\bar{E}). When \bar{E} is HIGH all

outputs are forced HIGH. The enable can be used as data input for a 4-output demultiplexer application.

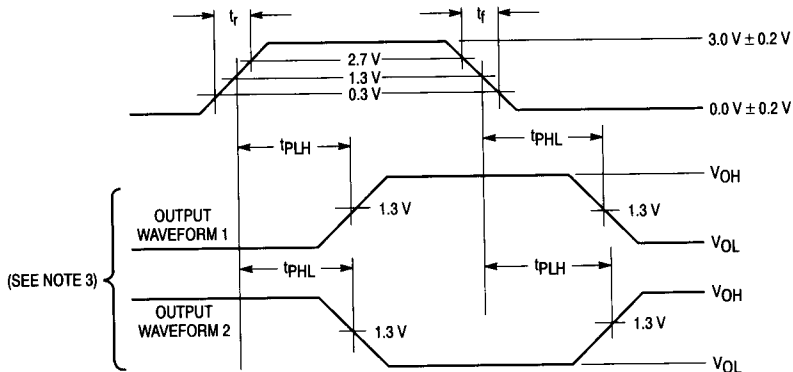
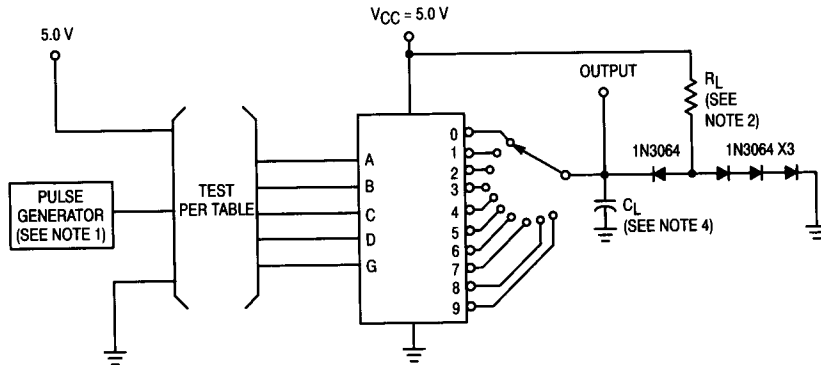
Each half of the 'LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions and thereby reducing the number of packages required in a logic network.

Pin Names	Loading (Note a)	
	HIGH	LOW
A_0-A_1 Address Inputs	0.5 U.L.	0.25 U.L.
\bar{E} Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
\bar{O}_1, \bar{O}_3 Active LOW Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

- a. One TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

TEST CIRCUIT AND WAVEFORM



NOTES:

1. The input pulse has the following characteristics:
 $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz and minimum duty cycle = 50%.
2. $R_L = 2.0$ k $\Omega \pm 10\%$.
3. Input-output waveform combination in accordance with truth table.
4. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance.
5. Voltage measurements are to be made with respect to network ground terminal.
6. All diodes are 1N3064 or equivalent.
7. The limits specified for $C_L = 15$ pF are guaranteed but not tested.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -0.4 mA, E _a = 2.0 V, other inputs are open.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V, V _{IH} = 2.0 V, E _a = 0.7 V.
V _{IC}	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V (all inputs).
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V (all inputs).
I _{IL}	Logical "0" Input Current	-0.12	-0.36	-0.12	-0.36	-0.12	-0.36	mA	V _{CC} = 5.5 V, V _{IN} = 0.4 V (all inputs).
I _{OS}	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (E _a), other inputs are open, V _{OUT} = GND.
I _{CC}	Power Supply Current Off		11		11		11	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), E _a = GND.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output High-Low	5.0 —	38 33	5.0 —	53 48	5.0 —	53 48	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PLH2} t _{PLH2}	Propagation Delay /Data-Output Low-High	5.0 —	25 20	5.0 —	35 30	5.0 —	35 30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PHL3} t _{PHL3}	Propagation Delay /Data-Output High-Low	5.0 —	37 38	5.0 —	52 47	5.0 —	52 47	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PLH3} t _{PLH3}	Propagation Delay /Data-Output Low-High	5.0 —	29 29	5.0 —	41 36	5.0 —	41 36	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PHL4} t _{PHL4}	Propagation Delay /Data-Output High-Low	5.0 —	43 32	5.0 —	60 55	5.0 —	60 55	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PLH4} t _{PLH4}	Propagation Delay /Data-Output Low-High	5.0 —	34 24	5.0 —	48 43	5.0 —	48 43	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.