



MOTOROLA

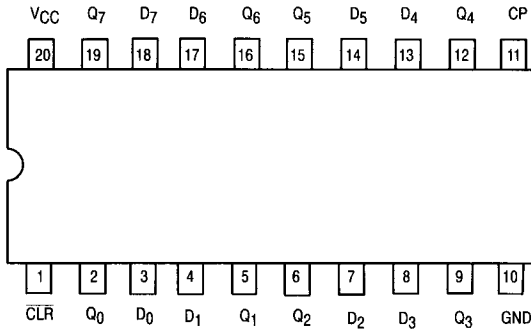
Octal D Flip-Flop With Common Clear

**ELECTRICALLY TESTED PER:
MIL-M-38510/32501**

The 54LS273 is a high-speed 8-Bit Register. The register consists of eight D type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset (CLEAR). This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- 8-Bit High-Speed Register
- Parallel Register
- Common Clock and Master Reset
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM



TRUTH TABLE			
CLR	CP	D _n	Q _n
L	X	X	L
H		H	H
H		L	L

H = HIGH Logic Level
L = LOW Logic Level
X = Immaterial

Military 54LS273



AVAILABLE AS:

- 1) JAN: JM38510/32501BXA
- 2) SMD: 7801001
- 3) 883: 54LS273/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2**

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

PIN ASSIGNMENTS

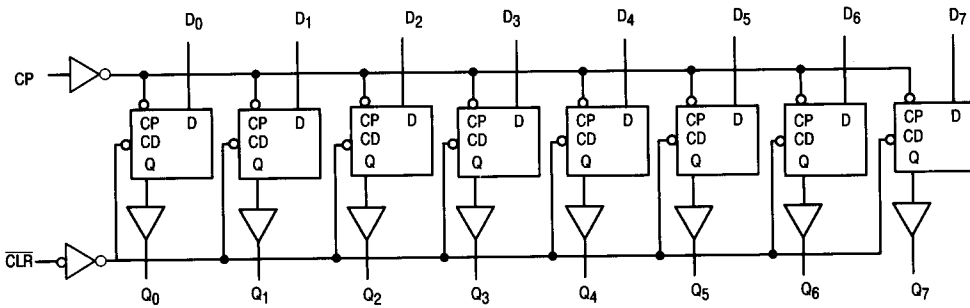
FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
CLR	1	1	1	GND
Q ₀	2	2	2	OPEN
D ₀	3	3	3	VCC
D ₁	4	4	4	VCC
Q ₁	5	5	5	OPEN
Q ₂	6	6	6	OPEN
D ₂	7	7	7	VCC
D ₃	8	8	8	VCC
Q ₃	9	9	9	OPEN
GND	10	10	10	GND
CP	11	11	11	VCC
Q ₄	12	12	12	OPEN
D ₄	13	13	13	VCC
D ₅	14	14	14	VCC
Q ₅	15	15	15	OPEN
Q ₆	16	16	16	OPEN
D ₆	17	17	17	VCC
D ₇	18	18	18	VCC
Q ₇	19	19	19	OPEN
VCC	20	20	20	VCC

BURN-IN CONDITIONS:

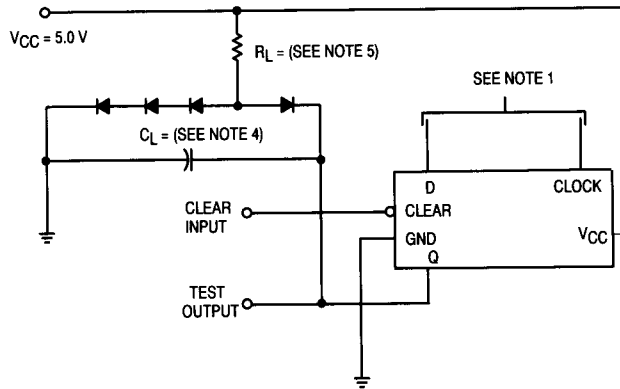
VCC = 5.0 V MIN/6.0 V MAX

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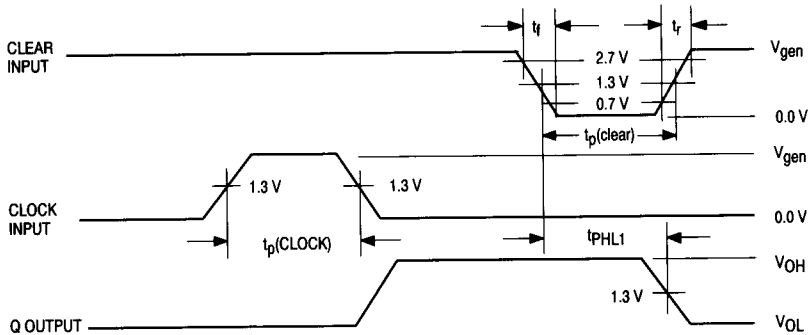
LOGIC DIAGRAM



AC TEST CIRCUIT



ASYNCHRONOUS SWITCHING WAVEFORMS

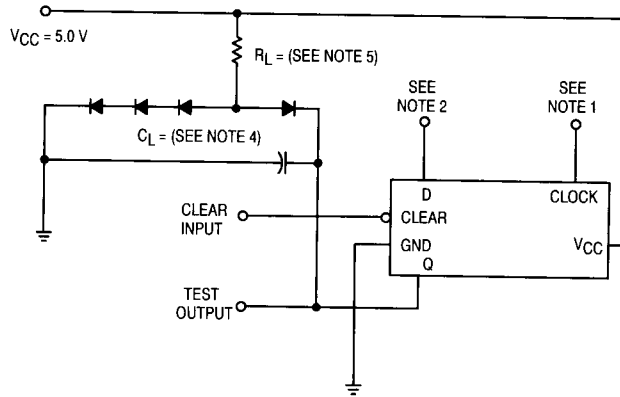


NOTES:

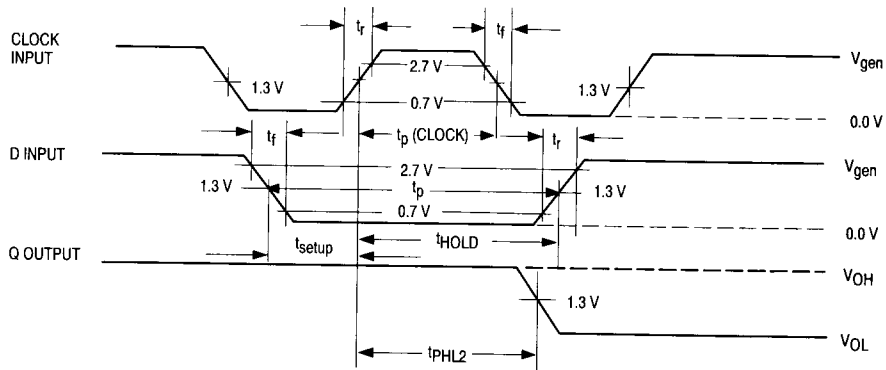
1. Clear input dominates regardless of the state of the clock or D inputs.
2. All diodes are 1N3064, or equivalent.
3. Clear input pulse characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_f \leq 6.0 \text{ ns}$, $t_r \leq 15 \text{ ns}$, $t_p(\text{clear}) = 20 \text{ ns}$ and $\text{PRR} \leq 1.0 \text{ MHz}$.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.
6. Clock input pulse characteristics: $t_p(\text{clock}) \geq 20 \text{ ns}$, $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$ and $\text{PRR} \leq 1.0 \text{ MHz}$.
7. Terminal conditions (pins not designated may be high $\geq 2.0 \text{ V}$, low $\leq 0.7 \text{ V}$, or open).

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SYNCHRONOUS SWITCHING (LOW-LEVEL DATA) TEST CIRCUIT



WAVEFORMS



NOTES:

1. Clock input pulse has the following characteristics:
 $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_p \text{ (clock)} = 30 \text{ ns}$ and $PRR \leq 1.0 \text{ MHz}$. When testing t_{MAX} , $PRR =$ (see table), $t_f = t_r \leq 6.0 \text{ ns}$.
2. D input has the following characteristics:
 $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_{setup} = 20 \text{ ns}$, $t_{hold} = 5.0 \text{ ns}$, $t_p = 25 \text{ ns}$ and PRR is 50% of the clock PRR . For t_{MAX} , $t_f = t_r \leq 6.0 \text{ ns}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.
6. Terminal conditions (pins not designated may be high $\geq 2.0 \text{ V}$, low $\leq 0.7 \text{ V}$, or open).

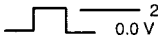
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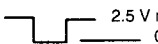
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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = - 0.4 mA, V _{IN} = 2.0 V, other inputs are open, \overline{CLR} = 2.0 V, CP = (See Note 1).
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, other inputs are open, \overline{CLR} = 2.0 V or 0.7 V, V _{IN} = 0.7 V, CP = (See Note 1).
V _{IC}	Input Clamping Voltage		- 1.5					V	V _{CC} = 4.5 V, I _{IN} = - 18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{IL}	Logical "0" Input Current	- 105	- 345	- 105	- 345	- 105	- 345	μA	V _{CC} = 5.5 V, V _{IL} (\overline{CLR}) = 0.4 V, other inputs are open.
I _{IL}	Logical "0" Input Current	- 160	- 400	- 160	- 400	- 160	- 400	μA	V _{CC} = 4.5 V, V _{IN} = 0.4 V, other inputs are open.
I _{OS}	Output Short Circuit Current	- 15	- 100	- 15	- 100	- 15	- 100	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, \overline{CLR} = 4.5 V, CP = (See Note 2).
I _{CC}	Power Supply Current		27		27		27	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), CP = (See Note 2).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

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NOTES:

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2.5 V minimum/5.5 V maximum
0.0 V
- 

2.5 V minimum/5.5 V maximum
0.0 V

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output CLR to Q _n	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output CP to Q _n	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH2} t _{PLH2}	Propagation Delay /Data-Output CP to Q _n	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
f _{MAX}	Maximum Clock Frequency	25		25		25		MHz	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%.
f _{MAX}	Maximum Clock Frequency	30						MHz	V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.

NOTE:

The limits specified for C_L = 15 pF are guaranteed, but not tested.