

SN74ALVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

The SN74ALVC16543 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16543 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1LEAB	2	55	1LEBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2CEAB	26	31	2CEBA
2LEAB	27	30	2LEBA
2OEAB	28	29	2OEBA

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TEXAS
INSTRUMENTS

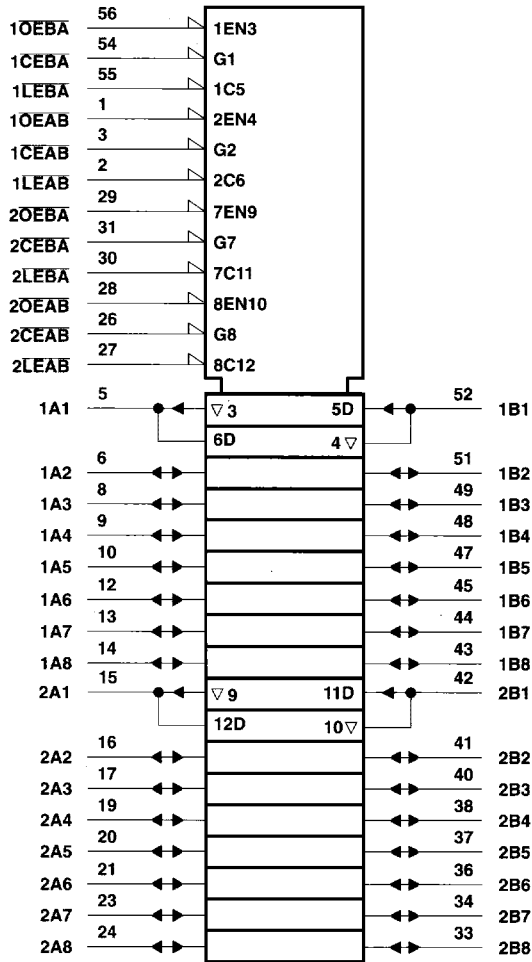
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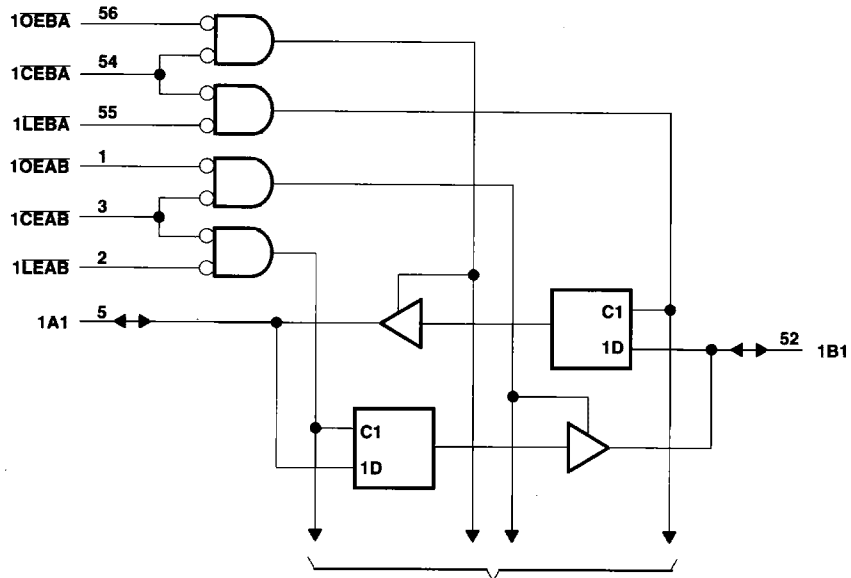
logic symbol†



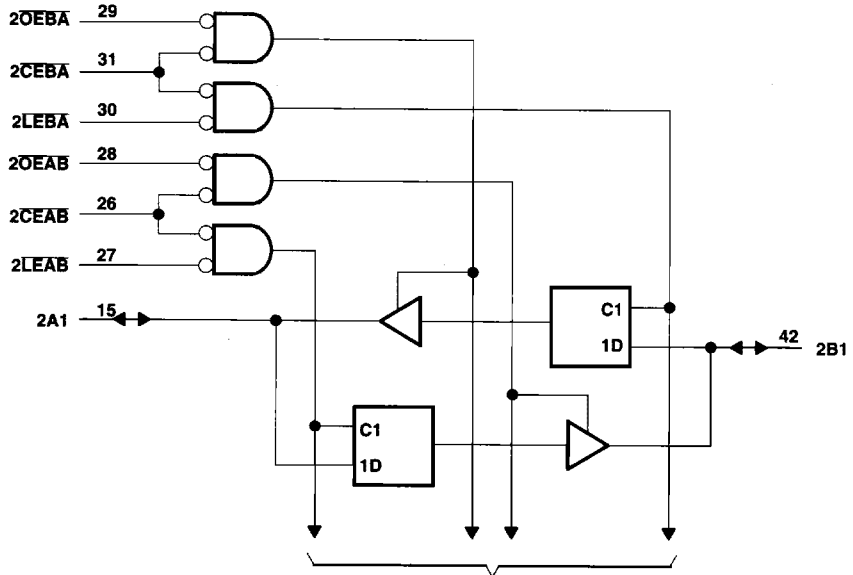
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



To 7 Other Channels



To 7 Other Channels

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FUNCTION TABLE†
 (each 8-bit section)

INPUTS				OUTPUT
CEAB	LEAB	OEAB	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

‡ Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [¶]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [¶]
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

[¶] Current duty cycle ≤ 50%, $f \geq 1$ kHz

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}		I _I = -18 mA	2.7 V			-1.2	V
V _{OH}		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
		I _{OH} = -12 mA	2.7 V	2.2			
			3 V	2.4			
V _{OL}		I _{OH} = -24 mA	3 V	2			V
		I _{OL} = 100 μA	MIN to MAX			0.2	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I		V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} [‡]		V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	TBD			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	TBD			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

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