

Product Features

- PI74AVC+16601 is designed for low-voltage operation, $V_{CC} = 1.65V$ to $3.6V$
- True $\pm 24mA$ Balanced Drive @ $3.3V$
- I_{OFF} supports partial power-down operation
- $3.6V$ I/O Tolerant Inputs and Outputs
- All outputs contain a patented DDC (Dynamic Drive Control) that reduces noise without degrading propagation delay.
- Industrial operation: $-40^{\circ}C$ to $+85^{\circ}C$
- Available Packages:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 173 mil wide plastic TVSOP (K)

Product Description

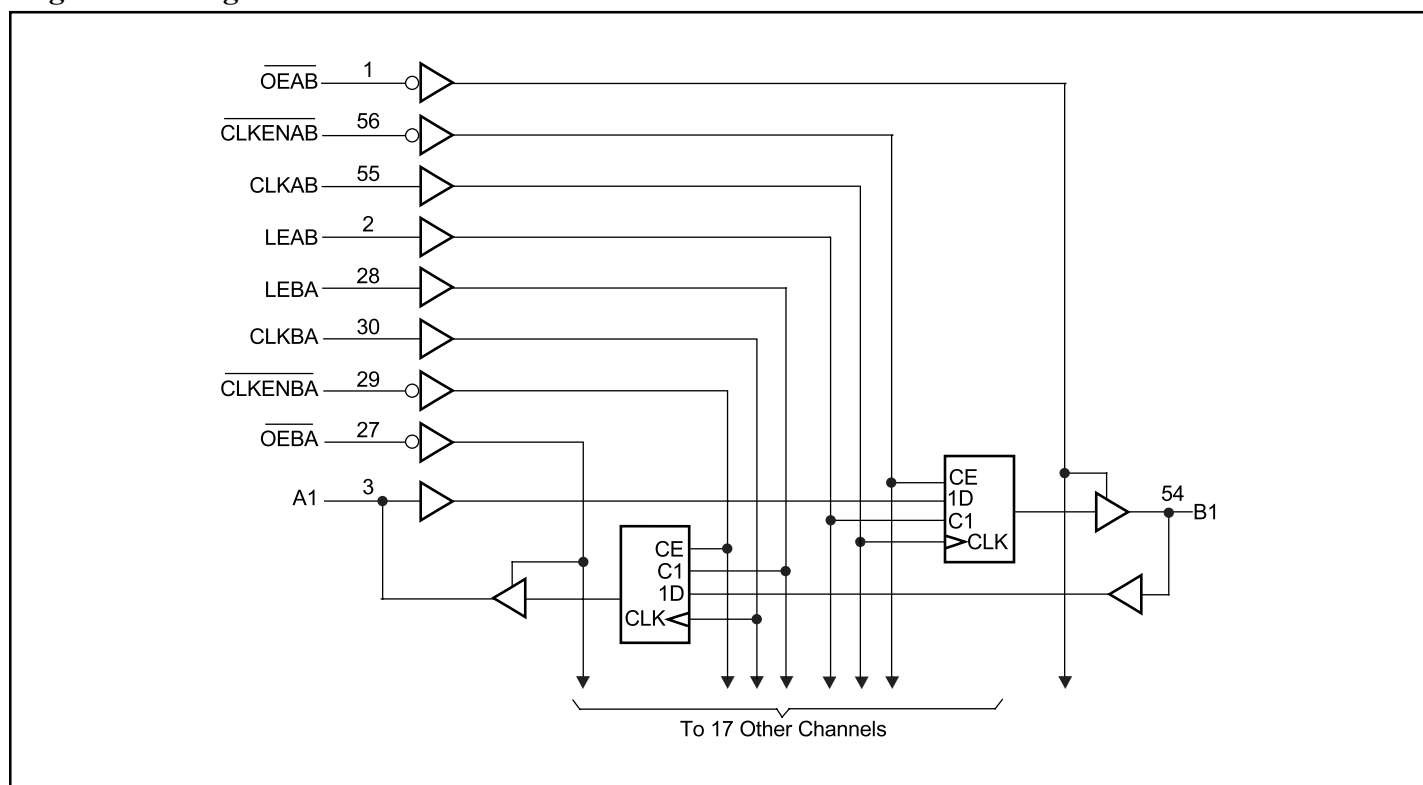
Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74AVC+16601 uses D-type latches and D-type flip-flops with 3-state outputs to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by Output Enable (\overline{OEAB} and \overline{OEBA}), Latch Enable (LEAB and LEBA), and Clock (CLKAB and CLKBA) inputs. The clock can be controlled by the Clock Enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is HIGH, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Logic Block Diagram


Pin Description

Pin Name	Description
\overline{OE}	Output Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
V _{CC}	Power

Pin Configuration

OEAB □ 1		56 □ CLKENAB
LEAB □ 2		55 □ CLKAB
A1 □ 3		54 □ B1
GND □ 4		53 □ GND
A2 □ 5		52 □ B2
A3 □ 6		51 □ B3
VCC □ 7		50 □ VCC
A4 □ 8		49 □ B4
A5 □ 9		48 □ B5
A6 □ 10		47 □ B6
GND □ 11		46 □ GND
A7 □ 12	56-Pin A,K	45 □ B7
A8 □ 13		44 □ B8
A9 □ 14		43 □ B9
A10 □ 15		42 □ B10
A11 □ 16		41 □ B11
A12 □ 17		40 □ B12
GND □ 18		39 □ GND
A13 □ 19		38 □ B13
A14 □ 20		37 □ B14
A15 □ 21		36 □ B15
VCC □ 22		35 □ VCC
A16 □ 23		34 □ B16
A17 □ 24		33 □ B17
GND □ 25		32 □ GND
A18 □ 26		31 □ B18
OEBA □ 27		30 □ CLKBA
LEBA □ 28		29 □ CLKENBA

Truth Table^{(1)†}

Inputs					Output B
CLKENAB	OEAB	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	S	H	H
H	L	L	X	X	B ₀ ‡
H	L	L	X	X	B ₀ ‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L or H	X	B ₀ ‡

Notes:

1. H = High Signal Level
 L = Low Signal Level
 Z = High Impedance
 ↑ = LOW-to-HIGH Transition

† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC}	-0.5V to +4.6V	Output clamp current, I_{OK} ($V_O < 0$)	-50mA
Input voltage range, V_I	-0.5V to +4.6V	Continuous output current, I_O	± 50 mA
Voltage range applied to any output in the high-impedance or power-off state, $V_O^{(1)}$	-0.5V to +4.6V	Continuous current through each V_{CC} or GND	± 100 mA
Voltage range applied to any output in the high or low state, $V_O^{(1,2)}$	-0.5V to $V_{CC} + 0.5$ V	Package thermal impedance, $\theta_{JA}^{(3)}$: package A	64°C/W
Input clamp current, I_{IK} ($V_I < 0$)	-50mA	package K	48°C/W
		Storage Temperature range, T_{stg}	-65°C to 150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. Input & output negative-voltage ratings may be exceeded if the input and output current rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽¹⁾

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	$V_{CC} = 1.2$ V	V_{CC}		
	$V_{CC} = 1.65$ V to 1.95V	$0.65 \times V_{CC}$		
	$V_{CC} = 2.3$ V to 2.7V	1.7		
	$V_{CC} = 3$ V to 3.6V	2		
V_{IL} Low-level Input Voltage	$V_{CC} = 1.2$ V		GND	
	$V_{CC} = 1.65$ V to 1.95V		$0.35 \times V_{CC}$	
	$V_{CC} = 2.3$ V to 2.7V		0.7	
	$V_{CC} = 3$ V to 3.6V		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	$V_{CC} = 1.65$ V to 1.95V		-6	mA
	$V_{CC} = 2.3$ V to 2.7V		-12	
	$V_{CC} = 3$ V to 3.6V		-24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V to 1.95V		6	
	$V_{CC} = 2.3$ V to 2.7V		12	
	$V_{CC} = 3$ V to 3.6V		24	
$\Delta t_{\Delta v}$ Input transition rise or fall rate	$V_{CC} = 1.65$ V to 3.6V		5	ns/V
T_A Operating free-air temperature		-40	85	°C

Notes:

1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$)

Parameters		Test Conditions ⁽¹⁾	V_{CC}	Min.	Max.	Units
V_{OH}		$I_{OH} = -100\mu\text{A}$	1.65V to 3.6V	$V_{CC} - 0.2\text{V}$		V
		$I_{OH} = -6\text{mA}$ $V_{IH} = 1.07\text{V}$	1.65V	1.2		
		$I_{OH} = -12\text{mA}$ $V_{IH} = 1.7\text{V}$	2.3V	1.75		
		$I_{OH} = -24\text{mA}$ $V_{IH} = 2\text{V}$	3V	2.0		
V_{OL}		$I_{OL} = 100\mu\text{A}$	1.65V to 3.6V		0.2	V
		$I_{OL} = 6\text{mA}$ $V_{IH} = 0.57\text{V}$	1.65V		0.45	
		$I_{OL} = 12\text{mA}$ $V_{IH} = 0.7\text{V}$	2.3V		0.55	
		$I_{OL} = 24\text{mA}$ $V_{IH} = 0.8\text{V}$	3V		0.8	
I_I	Control Inputs	$V_I = V_{CC}$ or GND	3.6V		± 2.5	μA
I_{OFF}		V_I or $V_O = 3.6\text{V}$	0		± 10	
I_{OZ}		$V_I = V_{CC}$ or GND	3.6V		± 10	
I_{CC}		$V_O = V_{CC}$ or GND $I_O = 0$	3.6V		40	
C_I	Control Inputs	$V_I = V_{CC}$ or GND	2.5V		4	pF
			3.3V		4	
	Data Inputs		2.5V		6	
			3.3V		6	
C_O	Outputs	$V_O = V_{CC}$ or GND	2.5V		8	
			3.3V		8	

Note:

1. Typical values are measured at $T_A = 25^{\circ}\text{C}$.

Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

		$V_{CC} = 1.2V$		$V_{CC} = 1.5V \pm 0.1V$		$V_{CC} = 1.8V \pm 0.15V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V \pm 0.3V$		Units	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
f_{clock}	Clock Frequency						150		250		350	MHz	
t_w	Pulse duration	LE high					3.3		2.0		1.5	ns	
		CLK high or low					3.3		2.0		1.5		
t_{su}	Setup time	Data before CLK \uparrow		3.5		2.5		2.0		1.9			1.5
		Data before LE \downarrow	CLK high	1.2		1.2		1.2		1.2			1.4
			CLK low	1.0		1.0		1.1		1.1			0.9
\overline{CLKEN} before CLK \uparrow		3.0		2.0		1.5		1.5		1.2			
t_h	Hold time	Data after CLK \uparrow		0		0		0.1		0.5		0.6	
		Data after LE \downarrow	CLK high	1.2		1.2		1.2		1.2		1.2	
			CLK low	2.3		1.7		1.7		1.7		1.5	
\overline{CLKEN} after CLK \uparrow		0		0		0.4		0.4		0.4			

Switching Characteristics

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

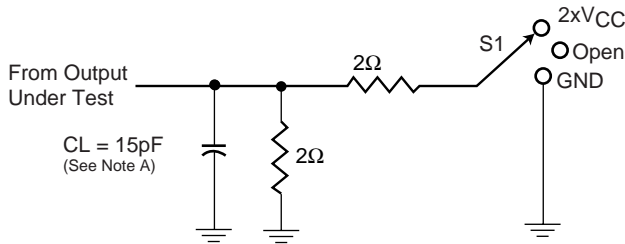
Parameter	From (Input)	To (Output)	$V_{CC} = 1.2V$		$V_{CC} = 1.5V \pm 0.1V$		$V_{CC} = 1.8V \pm 0.15V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V \pm 0.3V$		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{max}							150		250		350		MHz
t_{pd}	A or B	B or A		4.5		4.0		3.5		3.0		2.5	ns
	LEAB or LEBA	A or B		5.0		4.5		4.0		3.5		3.0	
	\overline{CLKAB} or \overline{CLKBA}			5.5		4.5		4.0		3.5		3.0	
t_{en}	\overline{OEAB} or \overline{OEBA}			4.5		4.0		4.0		3.5		3.0	
t_{dis}				5.5		4.0		4.0		3.0		3.0	

Operating Characteristics, $T_A = 25^\circ C$

Parameters		Test Conditions	$V_{CC} = 1.8V \pm 0.15V$	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Units
			Typical	Typical	Typical	
C_{pd} Power Dissipation Capacitance	Outputs Enabled	$C_L = 0pF,$ $f = 10 MHz$	22	26	30	pF
	Outputs Disabled		5	6	8	

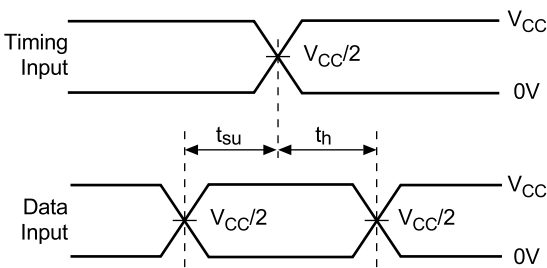
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2V \text{ and } 1.5V \pm 0.1V$

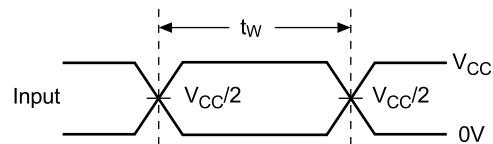


Load Circuit

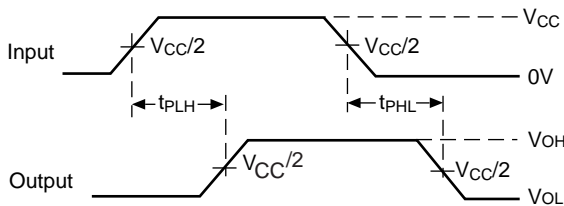
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



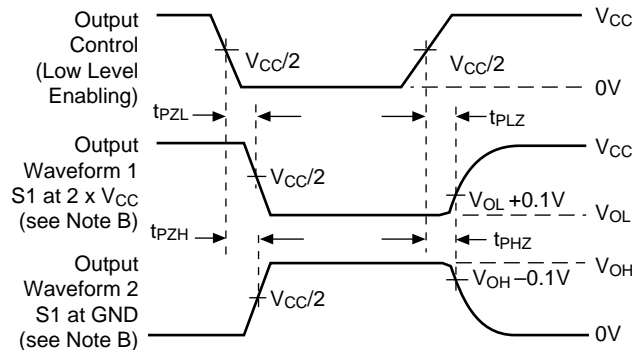
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

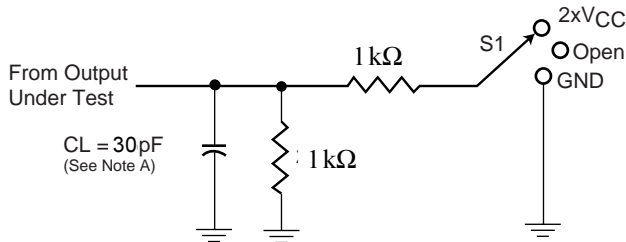
Figure 1. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0\text{ns}$, $t_F \leq 2.0\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. t_{PLH} and t_{PHL} are the same as t_{pd}

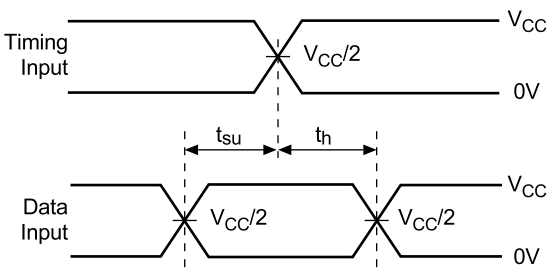
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8V \pm 0.15V$

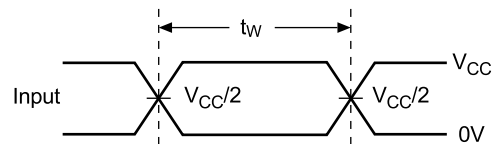


Load Circuit

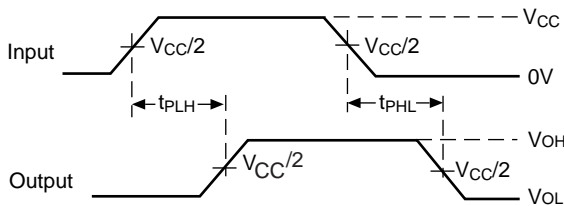
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



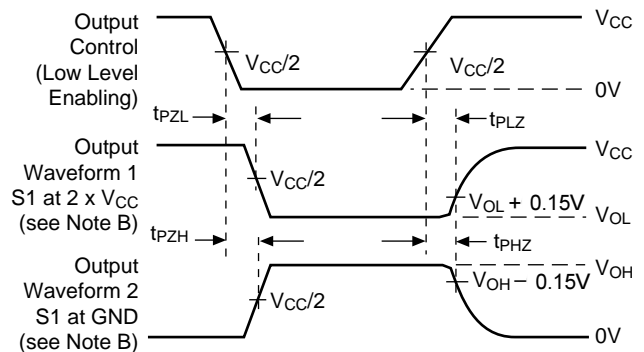
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

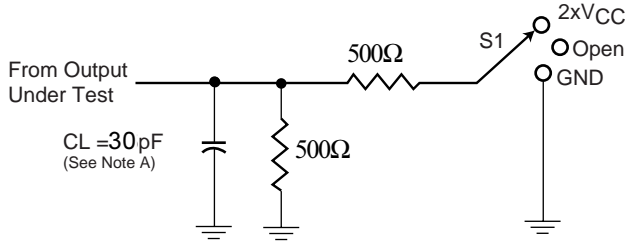
Figure 2. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0\text{ns}$, $t_F \leq 2.0\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. t_{PLH} and t_{PHL} are the same as t_{pd}

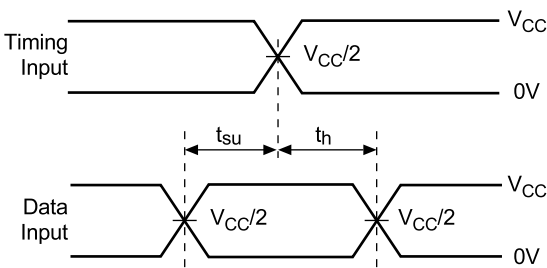
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5V \pm 0.2V$

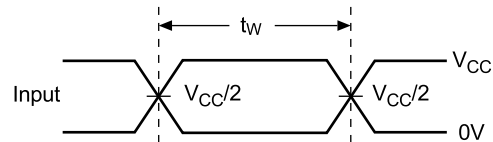


Load Circuit

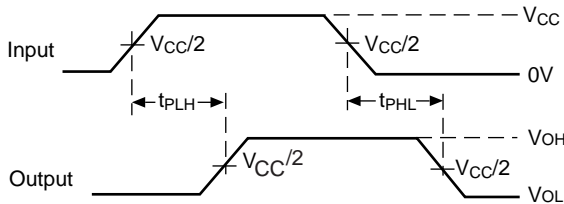
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



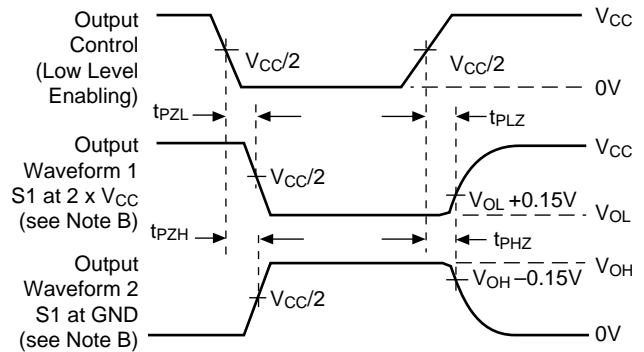
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

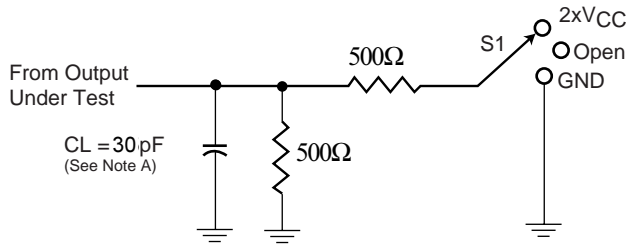
Figure 3. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0\text{ns}$, $t_F \leq 2.0\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. t_{PLH} and t_{PHL} are the same as t_{pd}

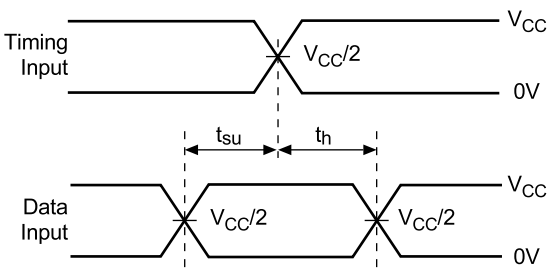
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3V \pm 0.3V$

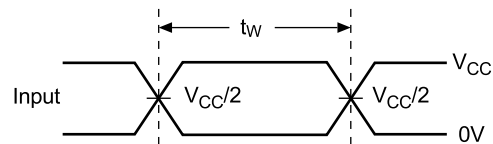


Load Circuit

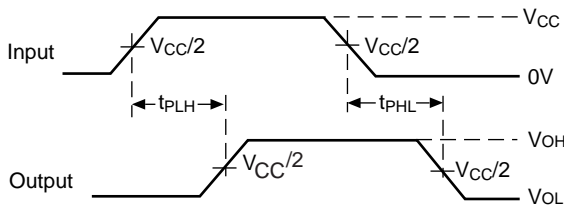
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



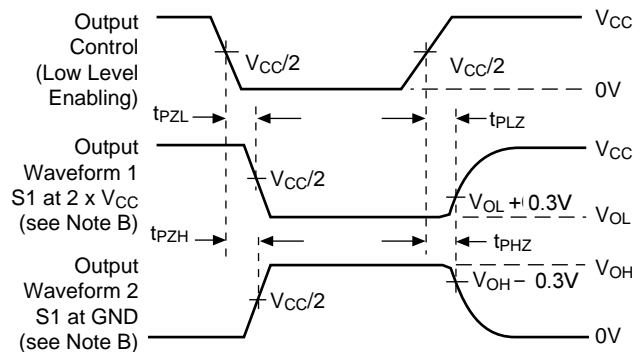
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



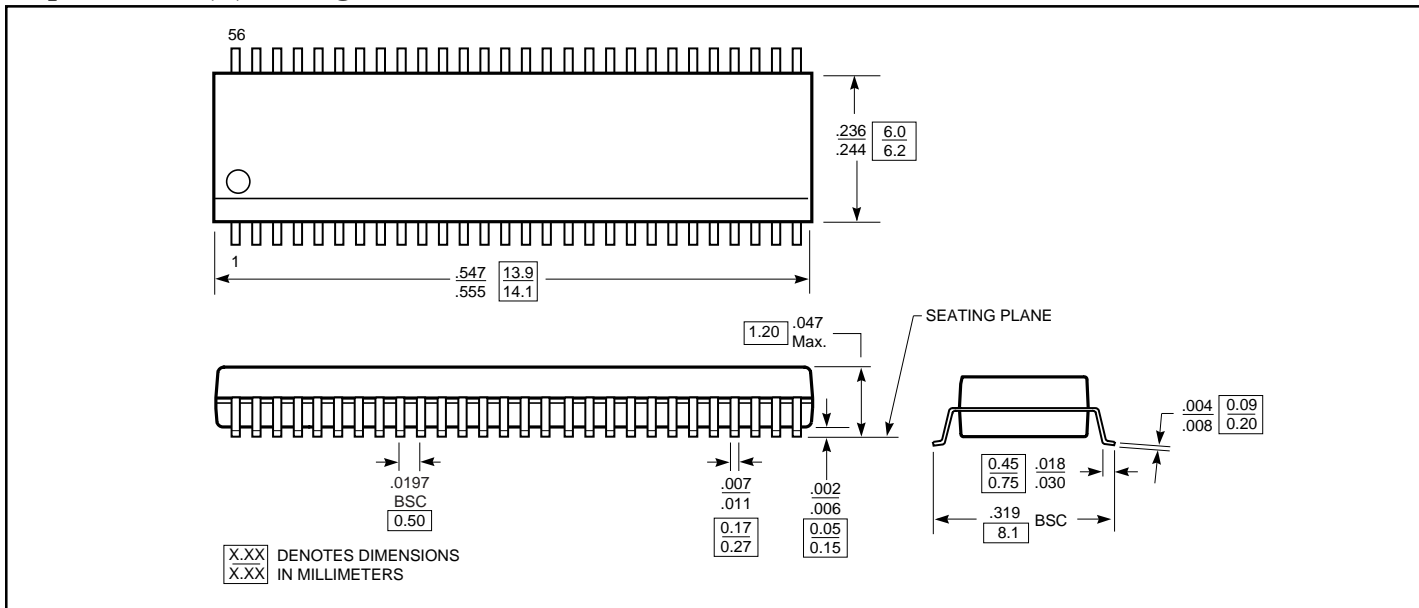
Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

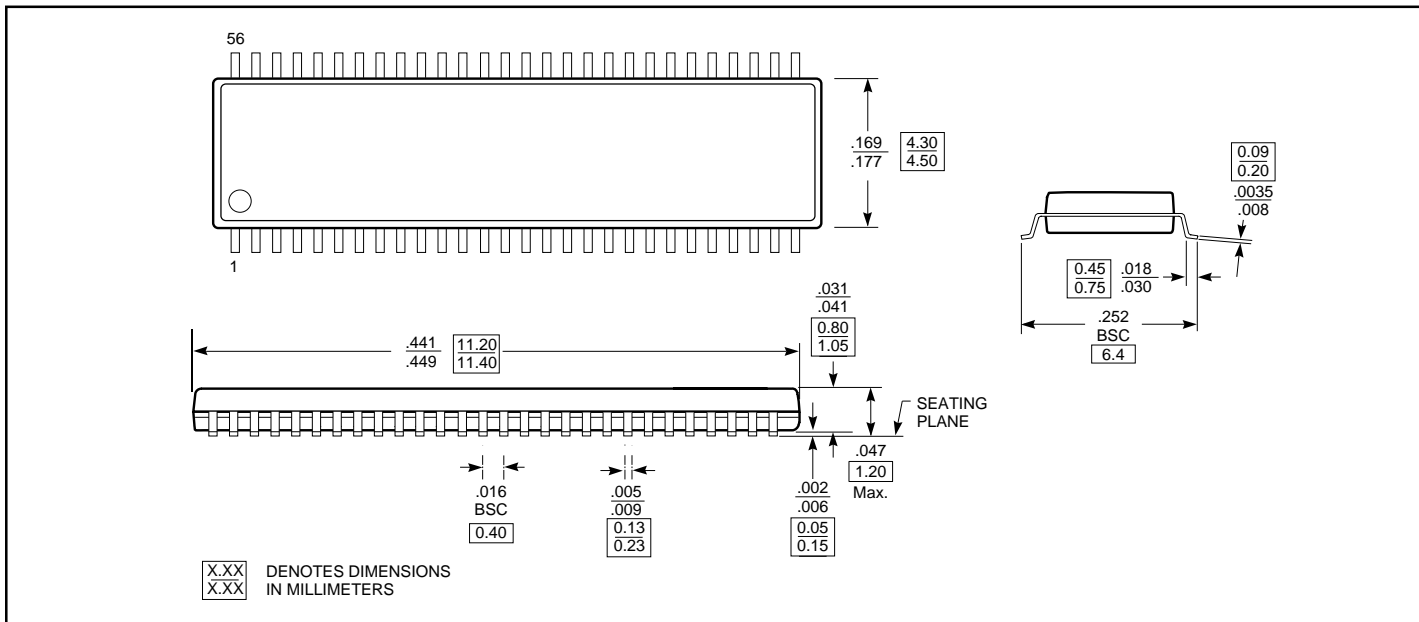
Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0\text{ns}$, $t_F \leq 2.0\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. t_{PLH} and t_{PHL} are the same as t_{pd}

56-pin TSSOP (A) Package



56-pin TVSOP (K) Package



Ordering Information

Ordering Data	Description
PI74AVC+16601A	56-pin, 240-mil wide plastic TSSOP
PI74AVC+16601K	56-pin, 173-mil wide plastic TVSOP