Signetics

Military Logic Products

54LS75
Latch

Quad Bistable Latch

Product Specification

FEATURES
- **4-bit bistable latch**

DESCRIPTION
The 54LS75 has four bistable latches. Each 2-bit latch is controlled by an active High Enable input (E). When E is High the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is High. The data on the D inputs one setup time before the High-to-Low transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is Low.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS75/BEA
16-Pin Ceramic FlatPack	54LS75/BFA
16-Pin Ceramic LLCC	54LS75/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

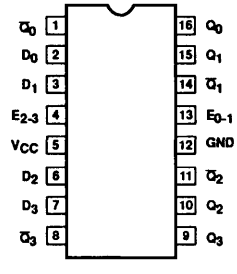
PINS	DESCRIPTION	54LS
D	Input	1LSUL
E	Input	4LSUL
All	Outputs	10LSUL

NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

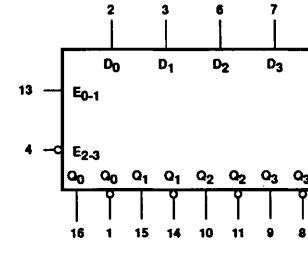
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

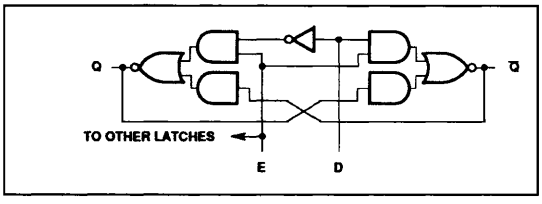
LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

Latch | 54LS75

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUT	
	E	D	Q	$\overline{Q}$
Data enabled	H H	L H	L H	H L
Data latched	L	X	q	$\overline{q}$

H = High voltage level
L = Low voltage level
X = Don't care
q = lower case letters indicate the state of referenced output one setup time prior to the High-to-Low Enable transition.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V	D inputs			0.1	mA
			E inputs			0.4	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	D inputs			20	µA
			E inputs			80	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	D inputs			-0.4	mA
			E inputs			-1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			6.3	12	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		27 17	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		20 15	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		27 25	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		30 15	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Enable pulse width	Waveform 3	20		ns
t_s	Setup time, data to enable	Waveform 4	20		ns
t_h	Hold time, data to enable	Waveform 4	5.0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		32 22	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		25 20	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		32 30	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		35 20	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		42 29	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		33 26	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		42 39	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		45.5 26.0	ns ns

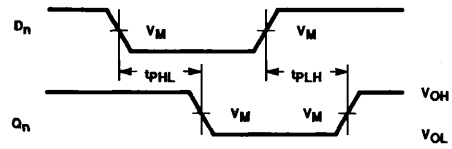
AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Enable pulse width	Waveform 3	20		ns
t_s	Setup time, data to enable	Waveform 4	20		ns
t_h	Hold time, data to enable	Waveform 4	5.0		ns

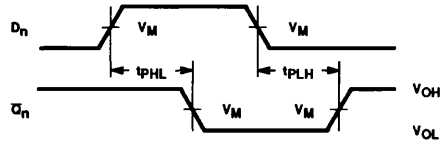
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

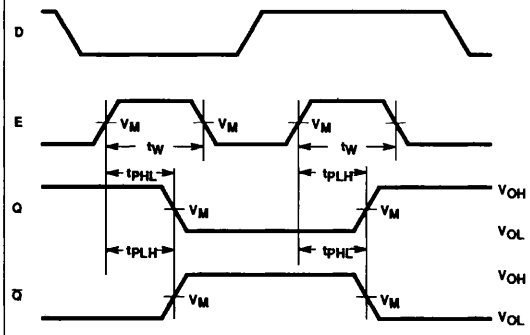
AC WAVEFORMS



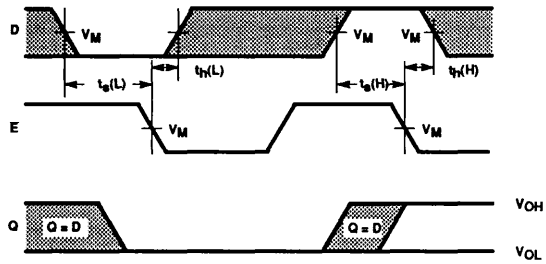
Waveform 1. Propagation Delay Data to Q Outputs



Waveform 2. Propagation Delay Data to $\overline{Q}$ Outputs



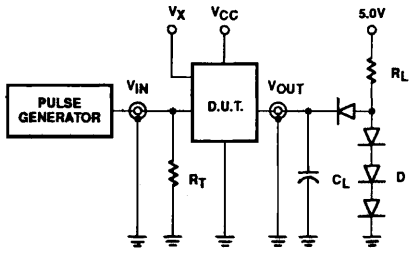
Waveform 3. Latch Enable to Output Delays and Latch Enable Pulse Width



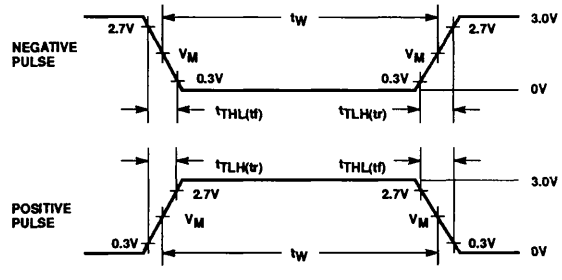
Waveform 4. Data Setup and Hold Times

NOTE: V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.