Octal D-type flip-flop with enable | 54ABT377

FEATURES

- Ideal for addressable register applications
- 8-bit positive edge triggered register
- Enable for address and data synchronization applications
- Output capability: +48mA/-24mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883D Method 3015.7 and 200V per Machine Model

DESCRIPTION

The 54ABT377 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT377 has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

ORDERING INFORMATION

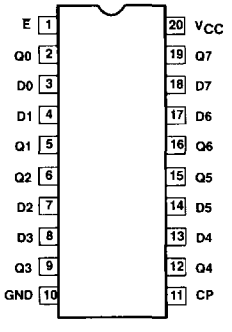
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54ABT377/BRA	GDIP1-T20
20-Pin Ceramic LLCC	54ABT377/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

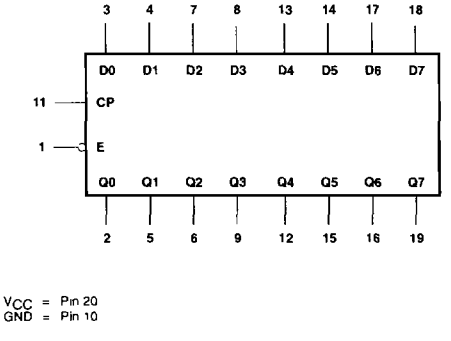
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{E}$	Enable input (active Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

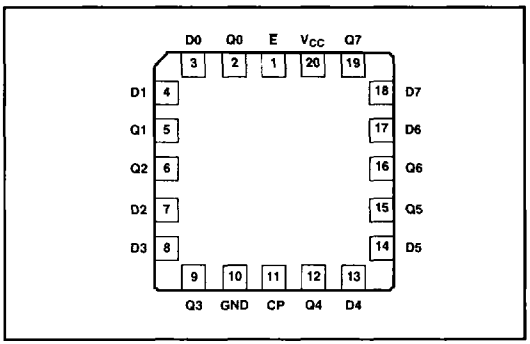


LOGIC SYMBOL

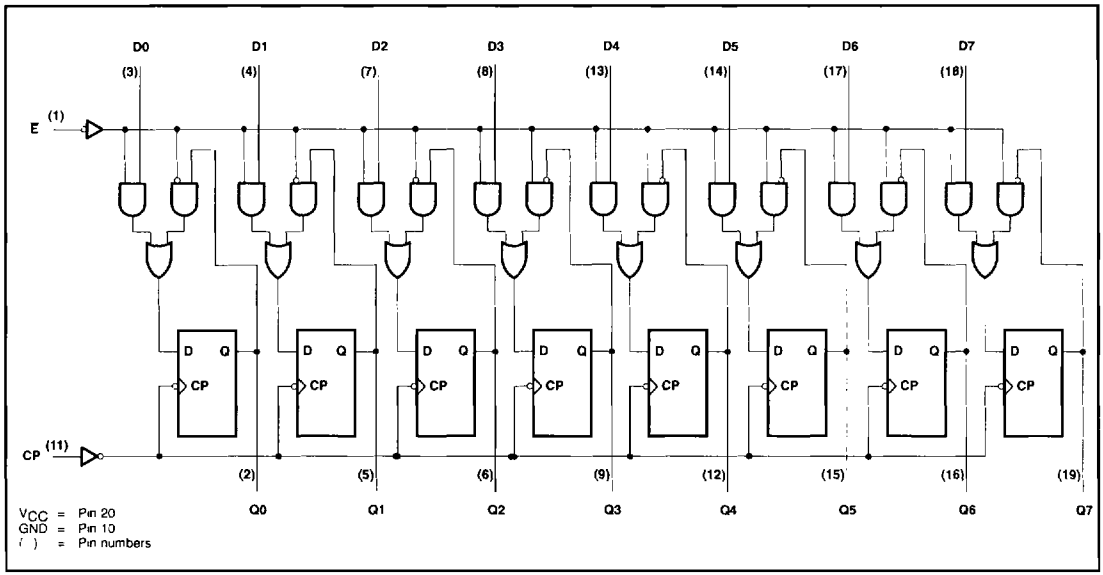


Octal D-type flip-flop with enable | 54ABT377

LLCC LEAD CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	INPUTS		OUTPUTS	OPERATING MODE
$\overline{E}$	CP	D_n	Q_n	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall time	0	5	ns/V
T_{amb}	Operating free-air temperature range	-55	+125	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage range[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	Output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	Output in Low state	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[3]	LIMITS		UNIT
			T_{amb} = -55 to 125°C		
			MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -3mA	2.5		V
		V_{CC} = 5.0V, I_{OH} = -3mA	3.0		V
		V_{CC} = MIN, I_{OH} = MAX	2.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = MAX		0.55	V
I_I	Input leakage current	V_I = GND or 5.5V		±1.0	µA
I_{OFF}	Power off leakage current	V_{CC} = 0V, V_I or $V_O \leq 4.5V$	-100	100	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V, V_O = 5.5V		50	µA
I_O	Output current[4]	V_O = 2.5V, V_I = GND or V_{CC}	-50	-180	mA
I_{CCH}	Quiescent supply current	Outputs High, V_I = GND or V_{CC}		250	µA
I_{CCL}		Outputs Low, V_I = GND or V_{CC}		30	mA
ΔI_{CC}	Additional supply current per input pin[5]	One input at 3.4V, other inputs at V_{CC} or GND		1.5	mA

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55 to 125°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.2 3.1	4.5 5.3	6.0 6.8	2.2 2.0	7.0 7.6	ns ns

AC SETUP REQUIREMENTS

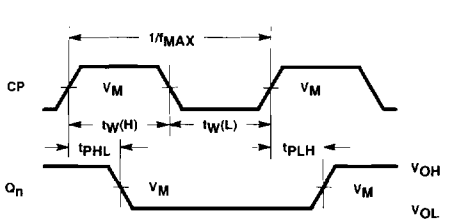
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55 to 125°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2[6]	2.0 2.0			2.5 2.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2[6]	1.8 1.8			1.8 1.8		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2[6]	3.0 3.0			3.0 3.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2[6]	1.0 1.0			1.8 1.8		ns ns
$t_w(H)$ $t_w(L)$	Clock Pulse width High or Low	Waveform 1[7]	3.3 3.3			3.3 3.3		ns ns

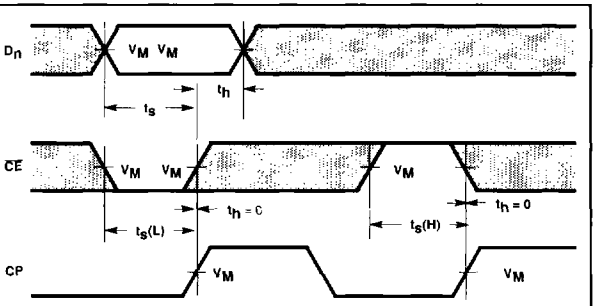
NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input ant output current ratings are observed.
3. V_{CC} = MAX, $V_I = V_{IL}$ or V_{IH}, unless otherwise noted.
4. Not more than one input should be tested at a time, and the duration of the test should note exceed one second.
5. This is the increase in supply current for each input at 3.4V.
6. t_{set} and t_{hold} limits that are less than 3.0ns are guaranteed, but are only tested to a 3.0ns limit due to tester limitations.
7. T_w limits that are less than 6.0ns are guaranteed, but are only tested to a 6.0ns limit due to tester limitations.

AC WAVEFORMS



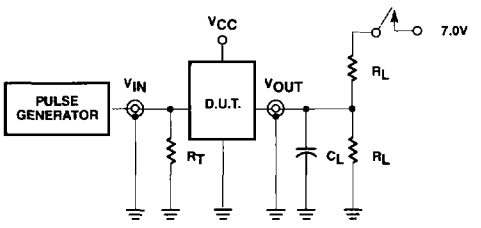
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



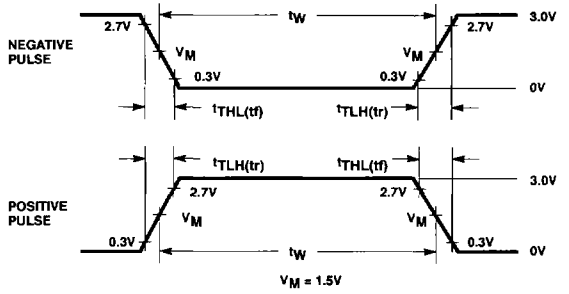
Waveform 2. Data and Enable Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

INPUT PULSE REQUIREMENTS					
Family	**Amplitude**	**Rep. Rate**	**t_W**	**t_R**	**t_F**
54ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = *Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.*