TC74AC563, 573 Octal D-Type Latch with 3-State Output

563: Inverting
573: Non-Inverting

Features:

- **High Speed:** t_{pd} = 6.0ns (typ.) at V_{CC} = 5V
- **Low Power Dissipation:** I_{CC} = 8μA (max.) at Ta = 25°C
- **High Noise Immunity:** $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- **Symmetrical Output Impedance:** $|I_{OH}| = I_{OL}$ = 24mA (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Wide Operating Voltage Range:** V_{CC} (opr)=2V~5.5V
- **Pin and Function Compatible with 74F563/573**
- **AC563 Available in DIP, SOIC and SOP Packages**
- **AC573 Available in DIP, SOIC, SOP, and SSOP Packages**

The TC74AC563 and TC74AC573 are advanced high speed CMOS OCTAL LATCHES with 3-STATE OUTPUTS fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

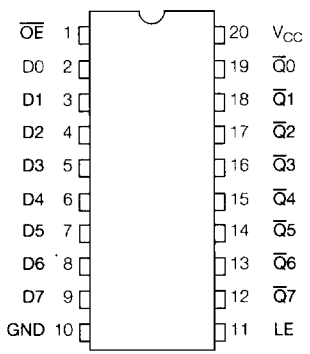
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74AC540 is an inverting type, and the TC74AC541 is a non-inverting type.

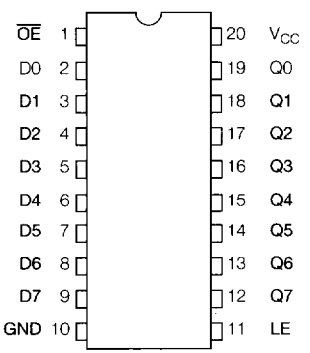
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Pin Assignment

TC74AC563



TC74AC563



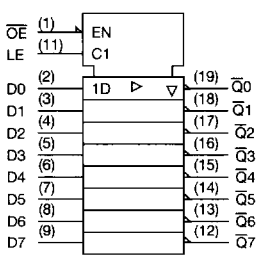
Truth Table

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(573)	$\overline{Q}$(563)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q}_n$
L	H	L	L	H
L	H	H	H	L

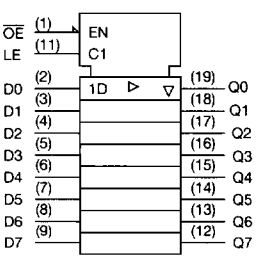
X: Don't Care
Z: High Impedance
Q_n ($\overline{Q}_n$): Q ($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

IEC Logic Symbol

TC74AC563



TC74AC573



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP) */180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 (V_{CC} = 3.3±0.3V) 0~20 (V_{CC} = 5±0.5V)	ns/v

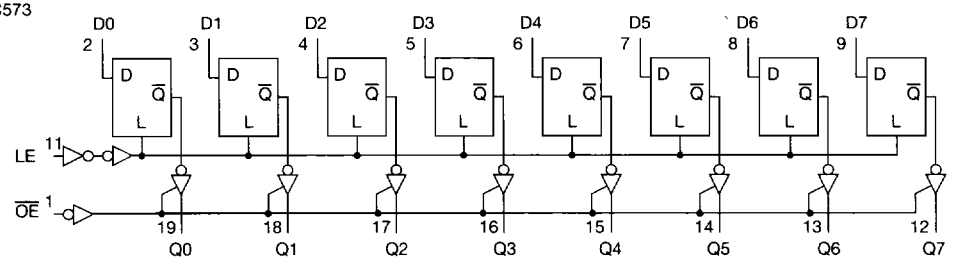
DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
				V_{CC}	Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-Level Input Voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = -4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} =12mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	

* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

System Diagram

TC74AC573



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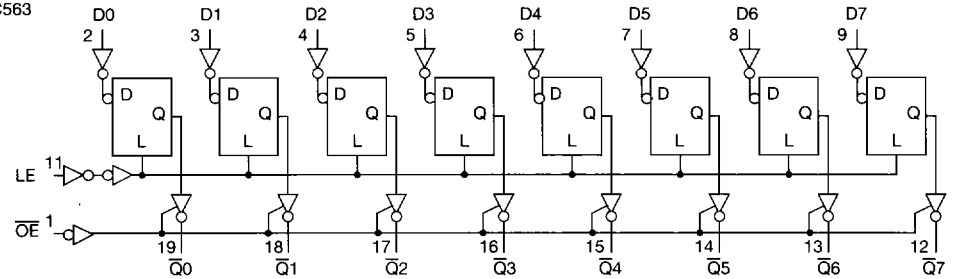

Timing Requirements (Input $t_r = t_f = 3n$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C		Ta= -40~85°	UNIT
			V_{CC}	Typ.	Max.	Max.	
Minimum Pulse Width (LE)	$t_{W(H)}$	—	3.3±0.3	—	7.0	7.0	ns
			5.0±0.5	—	5.0	5.0	
Minimum Set-up Time	t_s	—	3.3±0.3	—	7.0	7.0	
			5.0±0.5	—	4.0	4.0	
Minimum Hold Time	t_h	—	3.3±0.3	—	1.0	1.0	
			5.0±0.5	—	1.0	1.0	

AC Electrical Characteristics ($C_L = 50pF$, $R_L = 500\Omega$, Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Propagation Delay Time (LE–Q, $\overline{Q}$)	t_{pLH}	—	3.3±0.3	—	9.4	15.4	1.0	17.6	ns
	t_{pHL}		5.0±0.5	—	6.6	9.9	1.0	11.3	
Propagation Delay Time (Dn–Q, $\overline{Q}$)	t_{pLH}	—	3.3±0.3	—	9.4	16.0	1.0	18.2	
	t_{pHL}		5.0±0.5	—	6.2	8.9	1.0	10.2	
Output Enable Time	t_{pZL}	—	3.3±0.3	—	9.0	15.2	1.0	17.3	
	t_{pZH}		5.0±0.5	—	6.3	9.2	1.0	10.5	
Output Disable Time	t_{pLZ}	—	3.3±0.3	—	7.0	12.3	1.0	14.0	
	t_{pHZ}		5.0±0.5	—	6.0	8.8	1.0	10.0	
Input Capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Output Capacitance	C_{OUT}	—	—	—	10	—	—	—	
Power Dissipation Capacitance	C_{PD} [1]	—	—	—	32	—	—	—	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\ (opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC} / 8$ (per Latch). And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation: C_{PD} (total)=21+11 • n.