

Radiation Hardened Quad Differential Line Drivers

HS-26CT31RH, HS-26CT31EH

The Intersil HS-26CT31RH, HS-26CT31EH are quad differential line drivers designed for digital data transmission over balanced lines and meet the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CT31RH, HS-26CT31EH accept TTL signal levels and convert them to RS-422 compatible outputs. These circuits use special outputs that enable the drivers to power down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independently.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95632. A "hot-link" is provided on our homepage for downloading.

<http://www.landandmaritime.dla.mil/Downloads/MILSpec/Smd/95632.pdf>

Features

- Electronically Screened to SMD #5962-95632
- QML Qualified Per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened CMOS
- Total Dose Up to 300kRAD(Si)
- Latchup Free
- EIA RS-422 Compatible Outputs (Except for IOS)
- Operation with TTL Based on $V_{IH} = V_{DD}/2$
- High Impedance Outputs when Disabled or Powered Down
- Low Power Dissipation 2.75mW Standby (Max)
- Single 5V Supply
- Low Output Impedance 10Ω or Less
- Full -55°C to $+125^{\circ}\text{C}$ Military Temperature Range

Applications

- Line Transmitter for MIL-STD-1553 Serial Data Bus
- Line Transmitter for RS422

Ordering Information

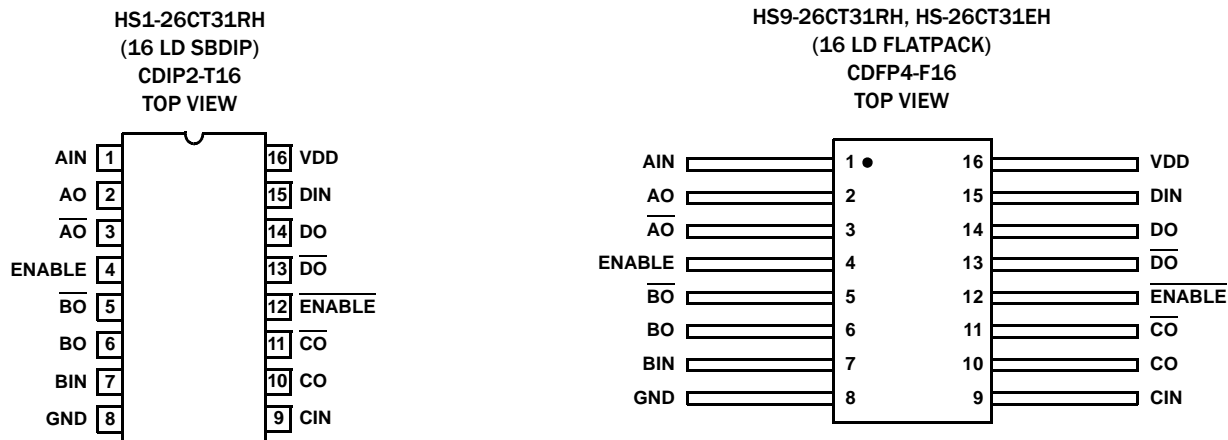
| ORDERING NUMBER (Note 1) | INTERNAL MKT. NUMBER | PART MARKING | TEMP. RANGE ($^{\circ}\text{C}$) | PACKAGE | PKG. DWG. # |
|--------------------------|------------------------------|-----------------------|------------------------------------|----------------|-------------|
| 5962F9563201QEC | HS1-26CT31RH-8 | Q 5962F95 63201QEC | -55 to +125 | 16 LD SBDIP | D16.3 |
| 5962F9563201QXC | HS9-26CT31RH-8 | Q 5962F95 63201QXC | -55 to +125 | 16 LD Flatpack | K16.A |
| 5962F9563201VEC | HS1-26CT31RH-Q | Q 5962F95 63201VEC | -55 to +125 | 16 LD SBDIP | D16.3 |
| 5962F9563201VXC | HS9-26CT31RH-Q | Q 5962F95 63201VXC | -55 to +125 | 16 LD Flatpack | K16.A |
| HS1-26CT31RH/PROTO | HS1-26CT31RH/PROTO | HS1 - 26CT31RH /PROTO | -55 to +125 | 16 LD SBDIP | D16.3 |
| HS9-26CT31RH/PROTO | HS9-26CT31RH/PROTO | HS9 - 26CT31RH /PROTO | -55 to +125 | 16 LD Flatpack | K16.A |
| 5962F9563201V9A | HS0-26CT31RH-Q | | -55 to +125 | Die | |
| 5962F9563202VXC | HS9-26CT31EH-Q | Q 5962F95 63202VXC | -55 to +125 | 16 LD Flatpack | K16.A |
| HS0-26CLV31RH/SAMPLE | HS0-26CLV31RH/SAMPLE | | -55 to +125 | Die | |
| 5962F9563201VYC | HS9G-26CT31RH-Q (Note 2) | Q 5962F95 63201VYC | -55 to +125 | 16 LD Flatpack | K16.A |
| HS9G-26CT31RH/PROTO | HS9G-26CT31RH/PROTO (Note 2) | HS9G-26CT31RH/PROTO | -55 to +125 | 16 LD Flatpack | K16.A |

NOTES:

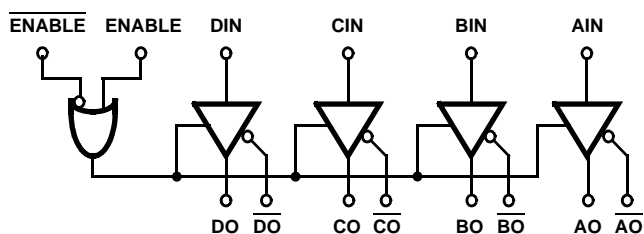
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The lid of these packages are connected to the ground pin of the device.

HS-26CT31RH, HS-26CT31EH

Pin Configurations



Logic Diagram



For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

HS-26CT31RH, HS-26CT31EH

Die Characteristics

DIE DIMENSIONS:

96.5 milx195 milsx21 mils
(2450x4950)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: $10\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Metallization:

M1: Mo/TiW
Thickness: 5800\AA
M2: Al/Si/Cu (Top)
Thickness: $10\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Substrate:

AVLSI1RA

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up):

V_{DD}

ADDITIONAL INFORMATION:

Worst Case Current Density:

$<2.0 \times 10^5 \text{A/cm}^2$

Bond Pad Size:

$110\mu\text{m} \times 100\mu\text{m}$

Metallization Mask Layout

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