8-Bit SERDE Pipeline Register

SN54/74S818

Features/Benefits

- High drive capability. I_{OL} = 32 mA (Com)
- Alternate source to Am29818
- Serial-parallel/Parallel-serial pipeline register
- Independent pathing and clocking controls
- Expandable in multiples of 8 bits
- Three-state outputs
- PNP inputs for low-inputcurrent
- 24-pin SKINNYDIP® saves space

Applications

- Universal interface element for systems using both serial and parallel data formats
- Serial communication and peripheral interface
- Microprogram control store output register
- Serial-parallel/Parallel-serial pipeline conversion
- State machine feedback path isolation/diagnostics
- Serial readback register

Description

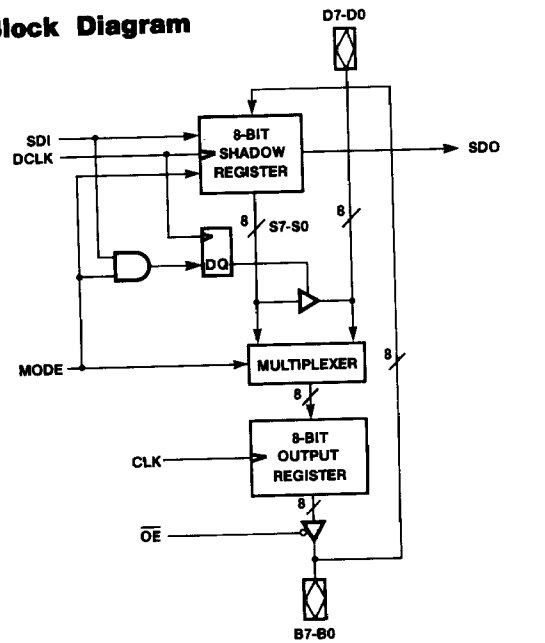
The SN54/74S818 is an 8-bit serializing/deserializing pipeline register. It can also be used as a serial readback register as well as a diagnostic register. All of these configurations are expandable in multiples of eight bits.

The 54/74S818 internally consists of a universal shift register and an 8-bit register. Its wide application results from a combination of powerful interconnection modes and independent clocking and pathing controls. It is ideally suited as a universal interface element involving both serial and parallel data formats.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S818	NS, JS, NL (28)	Com
SN54S818	JS, W, L (28)	Mil

Block Diagram



Function Table

INPUTS				OUTPUTS			OPERATION	SEE FIG.
MODE	SDI	CLK	DCLK	B7-B0	S7-S0	SDO		
L	X	↑	*	Bn ← Dn	HOLD	S7	Load output register from input bus	1
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S7	Shift shadow register data	2
L	X	↑	↑	Bn ← Dn	Sn ← Sn-1 S0 ← SDI	S7	Load output register from input bus while shifting shadow register data	1 & 2
H	X	↑	*	Bn ← Sn	HOLD	SDI	Load output register from shadow register	2,3,4
H	L	*	↑	HOLD	Sn ← Bn	SDI	Load shadow register from output bus	3
H	L	↑	↑	Bn ← Sn	Sn ← Bn	SDI	Swap shadow register and output register	
H	H	*	↑	HOLD	HOLD	SDI	Enable D7-D0 as outputs for RAM write-back	4

* Clock must be steady or falling.

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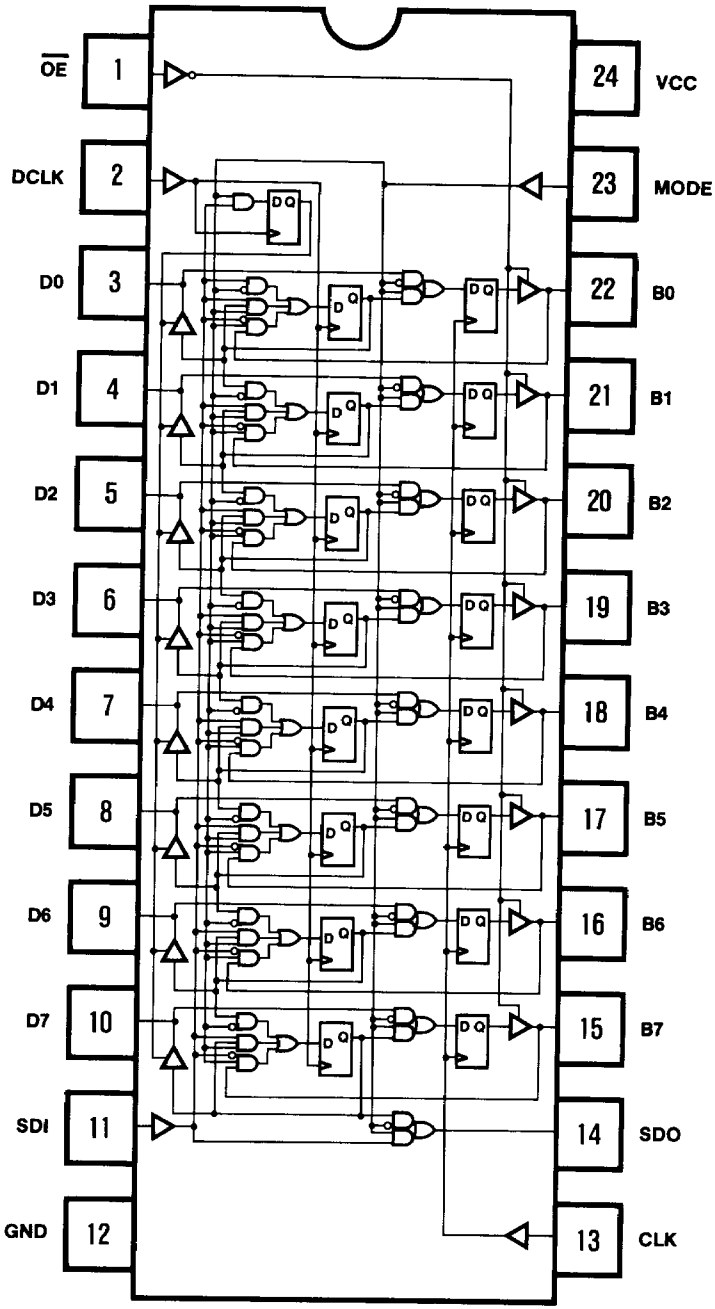
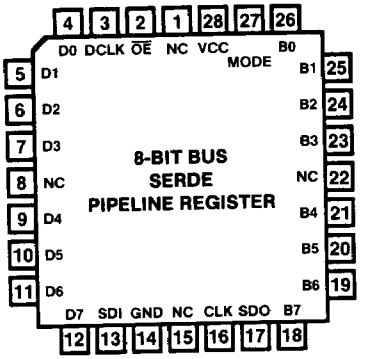
Logic Diagram



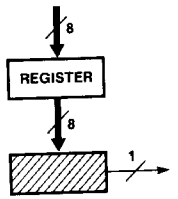
Pin Configuration

SN74S818

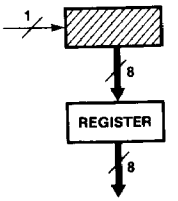


Plastic Chip Carrier

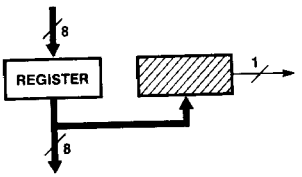
Typical Configurations



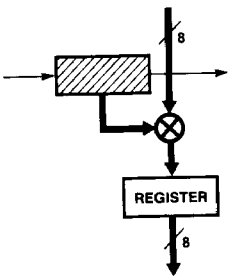
Serializing Pipeline Register



Deserializing Pipeline Register



Serial Readback Register



Diagnostic Register

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of CLK	High	15			12			ns
		Low	15			13			ns
t_{wd}	Width of DCLK	High	25			20			ns
		Low	25			20			ns
t_{suc}	Setup time from MODE to CLK		20↑			17↑			ns
t_{hc}	Hold time from CLK to MODE		0↑			0↑			ns
t_{sud}	Setup time from data to CLK		21↑			14↑			ns
t_{hd}	Hold time from CLK to data		0↑			0↑			ns
t_{sudc}	Setup time from SDI, MODE to DCLK		31↑			20↑			ns
t_{hdc}	Hold time from DCLK to SDI, MODE		0↑			0↑			ns
t_{sudq}	Setup time from output to DCLK		25↑			18↑			ns
t_{hdq}	Hold time from DLCK to output		0↑			0↑			ns

↑ ↓ The arrow indicates the transition of the clock/gate input used for reference: ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.2			−1.2	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.5 V			−0.25			−0.25	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			50			50	μA
I_I	Maximum input current	D or B	V_{CC} = MAX	V_I = 5.5 V			1			1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage	B7-B0	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 32 mA						0.5	V
				I_{OL} = 24 mA			0.5				
		SDO D7-D0		I_{OL} = 8 mA						0.5	
				I_{OL} = 4 mA			0.5				
V_{OH}	High-level output voltage	B7-B0	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = 6.5 mA	2.4			2.4			V
		SDO D7-D0		I_{OH} = −2 mA							
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.5 V			−250			−250	μA
I_{OZH}				V_O = 2.4 V			50			50	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX. Outputs open			115	155		115	145	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load/Waveforms)	MIN	MAX	UNIT
f_{MAX}	Maximum output clock frequency		C_L = 50 pF R_L = 280Ω $\overline{OE}$ = L	40		MHz
f_{MAXD}	Maximum diagnostic clock frequency	Cascaded	C_L = 50 pF R_L = 2 KΩ	20		MHz
		Uncascaded		25		
t_{CLK}	CLK to output delay		C_L = 50 pF R_L = 280Ω $\overline{OE}$ = L		14	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		C_L = 50 pF R_L = 2 KΩ		12	ns
t_{MS}	MODE to SDO delay				17	ns
t_{DS}	DCLK to SDO delay (MODE = LOW)				28	ns
t_{DEZL}	DCLK to D7-D0 enable delay		C_L = 50 pF R_L = 2 KΩ		25	ns
t_{DEZH}					20	ns
t_{DDLZ}	DCLK to D7-D0 disable delay		C_L = 5 pF R_L = 2 KΩ		36	ns
t_{DDHZ}					60	ns
t_{DC}	DCLK to CLK separation		C_L = 50 pF R_L = 280Ω $\overline{OE}$ = L	22		ns
t_{CD}	CLK to DCLK separation			35		ns
t_{PZL}	Output enable delay		C_L = 50 pF R_L = 280Ω		19	ns
t_{PZH}					13	ns
t_{PLZ}	Output disable delay		C_L = 5 pF R_L = 280Ω		12	ns
t_{PHZ}					22	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER		TEST CONDITIONS (See Interface Test Load/Waveforms)	MILITARY MIN	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum output clock frequency		C_L = 50 pF R_L = 280Ω OE = L	33		40		MHz
f_{MAXD}	Maximum diagnostic clock frequency	Cascaded	C_L = 50 pF R_L = 2 KΩ	16		20		MHz
		Uncascaded		20		25		
t_{CLK}	CLK to output delay		C_L = 50 pF R_L = 280Ω OE = L		18		14	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		C_L = 50 pF R_L = 2 KΩ		18		15	ns
t_{MS}	MODE to SDO delay				27		18	ns
t_{DS}	DCLK to SDO delay (MODE = LOW)				38		30	ns
t_{DEZL}	DCLK to D7-D0 enable delay		C_L = 50 pF R_L = 2 KΩ		35		25	ns
t_{DEZH}					30		25	ns
t_{DDLZ}	DCLK to D7-D0 disable delay		C_L = 5 pF R_L = 2 KΩ		45		45	ns
t_{DDHZ}					90		80	ns
t_{DC}	DCLK to CLK separation		C_L = 50 pF R_L = 280Ω OE = L	30		30		ns
t_{CD}	CLK to DCLK separation			45		40		ns
t_{PZL}	Output enable delay		C_L = 50 pF R_L = 280Ω		25		20	ns
t_{PZH}					20		15	ns
t_{PLZ}	Output disable delay		C_L = 5 pF R_L = 280Ω		20		15	ns
t_{PHZ}					30		25	ns

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Timing Waveforms

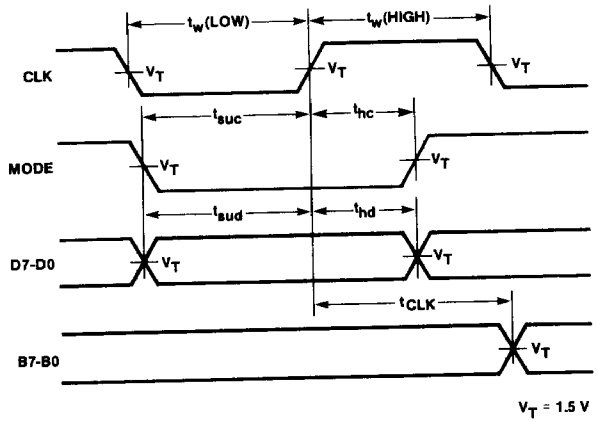

Figure 1. Switching waveforms for typical register applications ($\overline{OE}$ = L)

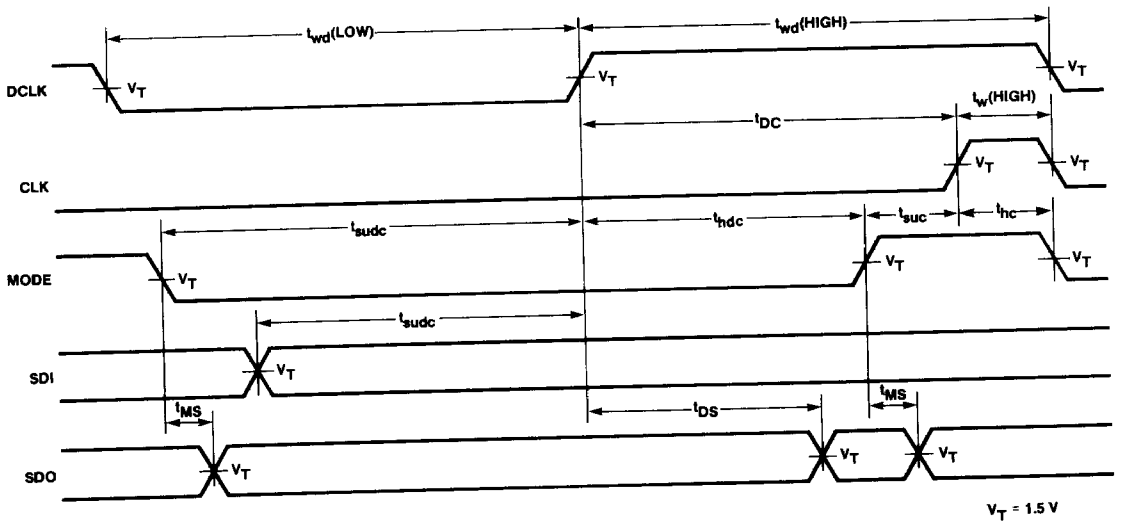

Figure 2. Switching waveforms for shift-in followed by diagnostic load

Timing Waveforms

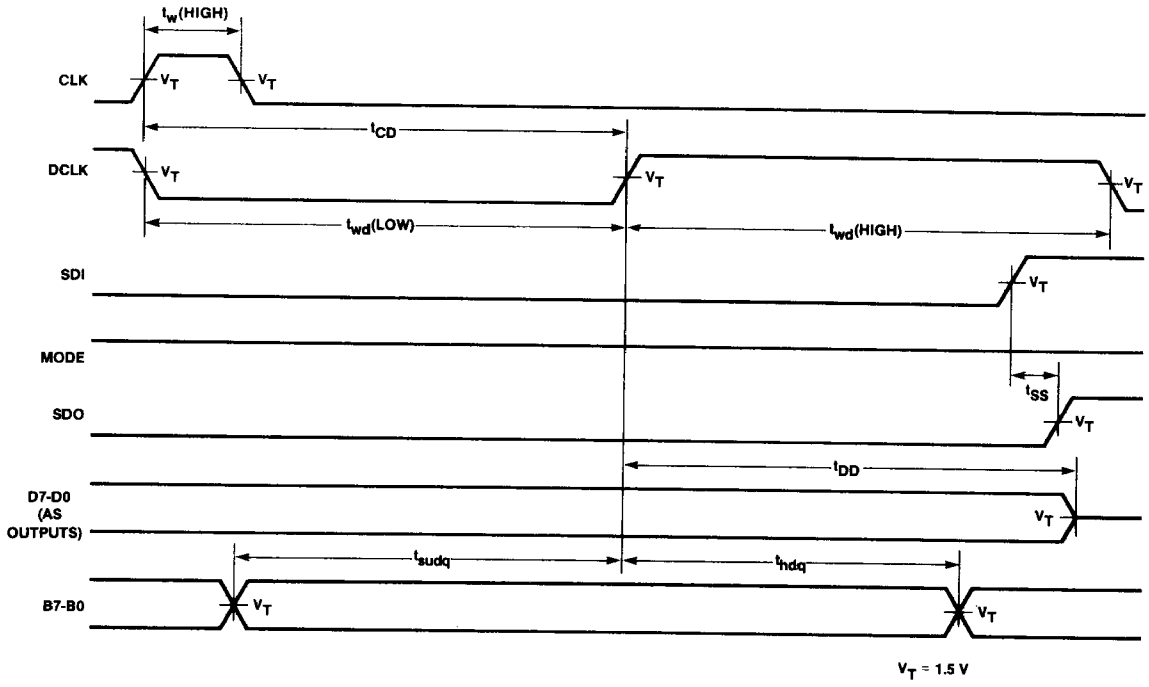

Figure 3. Switching waveforms for data bus (D7-D0) disabling

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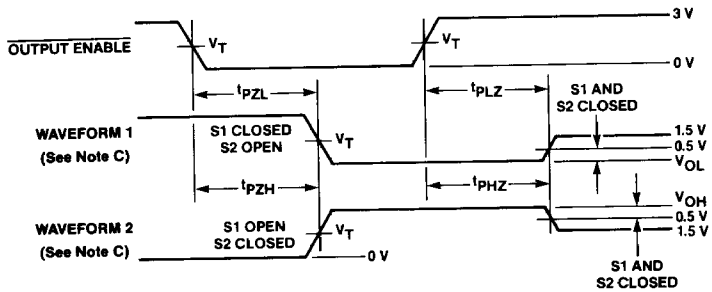
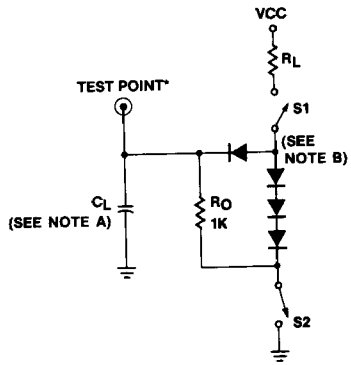
Enable/Disable Delay



Test Load



* The "TEST POINT" is drived by the output under test, and observed by instrumentation.

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz Z_{out} = 50Ω and for series 54/74S t_R = 2.5 ns t_F ≤ 2.5 ns.

F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

	B7-B0	D7-D0, SDO
R_O	1 KΩ	5 KΩ

Basics of Diagnostics

The basic theory of diagnostics is to insert test data to the inputs of a typical system and sample the test results from certain nodes of the circuits. For a combinatorial circuit, testing is very easy since the circuit has no memory of the previous states. But for a sequential circuit, the data to be sampled at a node depends not only on the inputs, but also on the current state it is in. If the previous state contains some error, it will possibly perform an illegal jump. In that case, depending on which state the system is currently in, the next state may be different. After several illegal jumps, it will be quite impossible to keep track of the jumps which it performs.

A way to solve the problem is by converting a sequential circuit to a combinatorial one. A sequential circuit can often be viewed as a network with a clock and a number of inputs and outputs, with some outputs being routed back to the inputs (see Figure 5a). If the loop is broken and inputs which are fed back from the outputs are instead fed in from some external sources (see Figure 5b), the system can be viewed as combinatorial and system testing will be easier. The "shadow register" concept involves shifting in serial data to the hidden register (the shadow register) and then loading test data to the output register. Together with other system inputs, the test results will appear on the output end of the network and can be sampled and analyzed. and analysed.

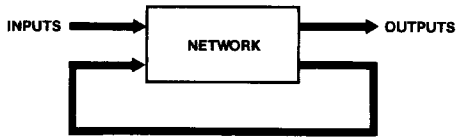


Figure 5a. A typical digital system

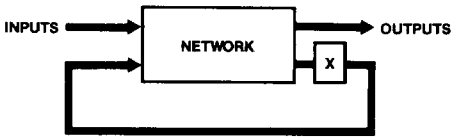


Figure 5b. The feedback of figure 5a is broken to convert the system to a non-sequential one

Diagnostic On-Chip™ (DOC™) Using Shadow Register

The diagnostic register is an 8-bit register with two levels of registers—a shadow register and an output register. A shadow register is basically a buried register with shift capability. There is also an output register whose outputs appear to the rest of the system. There is an output flipflop to each shadow flipflop. An output flipflop drives a three-state output buffer before going to the output pin. If the output is disabled, the output pin may be converted to an input pin. This feature is very important if the output is driving a bus and sampling of data on the bus is desired.

The input to a bit of the shadow register is a multiplexer which can select from one of the following nodes:

a) Output of the preceding bit of the shadow register (or SDI for the least significant bit).
b) Output of the same bit of the shadow register.
c) Data on the output pin of the same bit. This data may be the output of the corresponding bit of the output register if there is no output enable pin and the output is enabled, or the input to that pin if there is an output enable pin and output is disabled. Refer to Figure 6 for some general information on a typical diagnostic functional part with output enable ($\overline{OE}$).

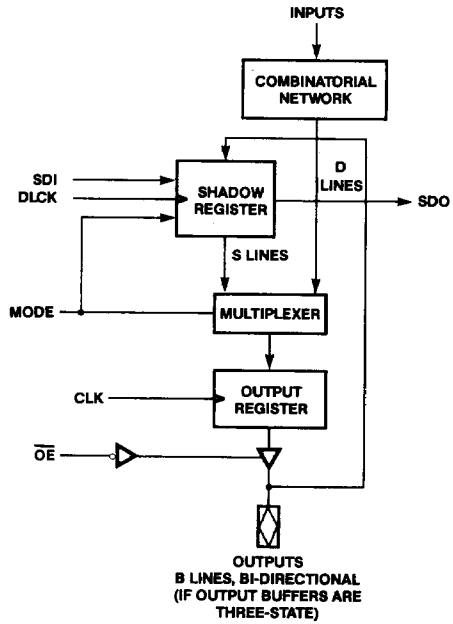


Figure 6. A typical functional block diagram for a diagnostic part

The input to any bit of the output register is also selected from one of the following nodes:
a) Corresponding input bit.
b) Corresponding output bit of the shadow register.

The reasons why a shadow register is preferred, as compared to shifting in diagnostic data directly to the output register, are:
a) The output register contains control signals for the system. Certain bits of this register may control different ports which are driving the same bus. As diagnostic data is shifted in, these bits become random and the ports they are controlling may drive a bus simultaneously. Invalid data may appear and worst of all, with a low-impedance path between the power supply, severe damage may be done to these ports.
b) As a diagnostic word is shifted in, the system is performing different tasks from what it is supposed to do. For example, when an ALU is performing an addition, diagnostic data is shifted in. The ALU then performs some other functions. The status of the system keeps changing. In some cases, illegal states may appear which produces unpredictable test results; for example, a flag may appear unpredictably.
c) The shadow register enables diagnostic data to be shifted in as background data without holding up the processor operation.

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The diagnostic register is one part in a series of diagnostic products which follows a new standard for diagnostics. The basic standard is described in Figure 6 and the table on page one. This standard implies that all diagnostic parts in this series are cascadable.

Diagnostic Pins

There are several pins in the diagnostic register in addition to the regular 8-bit inputs and outputs:

1) Diagnostic Clock (DCLK)—The diagnostic clock is used to clock the shadow register.

2) MODE—This pin is used in selecting the data to the registers. For the output register, MODE = LOW indicates that the output register is being used as a normal register; MODE = HIGH means that the next state of the output register will be obtained from the shadow register. For the shadow register, MODE = LOW indicates serial data from SDI (see below) is shifted in every diagnostic clock; MODE = HIGH switches SDI from a data input to a control input. See below for details.

3) Serial Data In (SDI)—When MODE = LOW, this pin is for shifting serial data in. When MODE = HIGH, SDI serves as a control pin. If MODE = HIGH and SDI = LOW, data from the output pins will be loaded to the shadow register on the next DCLK. MODE = HIGH and SDI = HIGH indicate a reserved operation. The data from the diagnostic clock is held the same. This reserved operation will be very significant when more operations than what is described are needed. The diagnostic register gives an example of how it can be used.

4) Serial Data Out (SDO)—When MODE = LOW, this pin carries the shift-out bit of the shadow register. When MODE = HIGH, the SDI becomes a control pin and the control signal should be passed along if several diagnostic parts are connected together serially. So SDO should carry SDI along in this case.

Write-Back to RAMs

Due to the applications of a diagnostic register in a writable microprogram control store, this part also includes an additional feature to initialize the control RAMs; when necessary, the input data pins to the register can be operated as output pins. In short, a diagnostic register is an 'asymmetric register transceiver' with shift capability. The term 'asymmetric register transceiver' means that there are two bidirectional registered ports on a chip, and these ports are enabled with different methodologies and have different timings. One port is still primarily for inputs (D7-D0), while the other is primarily for outputs (B7-B0).

When MODE and SDI are both HIGHs, the D7-D0 will be converted to an output port on the rising edge of the next DCLK by enabling the three-state buffers driving the D7-D0. The input for the three-state buffers is from the outputs of the shadow register (S7-S0).

Applications

This part can be used as a: microprogram control store register, data register, status register, address register, instruction register, interrupt mask register, interrupt vector, program counter, stack pointer, and for other general purposes.

If the diagnostic registers are used in a system using microprogram control words, status registers, and instruction registers, etc., one way to connect them together is shown in Figure 7. There is only one data input and one data output to the diagnostic parts. When serial data is shifted in or shifted out, data has to be passed from one diagnostic chip to another. Since SDI must be passed from chip-to-chip if it is used for control, it is necessary for logic designers to make sure the fall-through time of SDI to the last chip and the setup time from SDI to DCLK are satisfied.

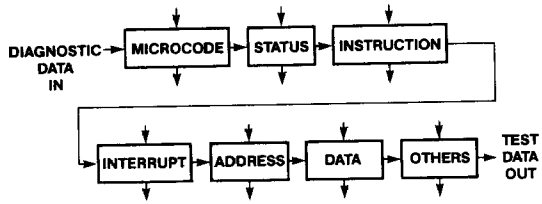

Figure 7. One way diagnostic registers can be linked together

The diagnostic registers are basically used for diagnostic purposes, although they may also function as parallel-to-serial and serial-to-parallel converters.

Two examples of how the diagnostic parts can be built into a system are shown in Figures 8, 9. The diagnostic registers are used to substitute the instruction register, memory data registers, status register, memory address registers, and the registers for a non-writable (Figure 8) or a writable (Figure 9) microprogram control store. The only additional block to a typical system without diagnostic features is the diagnostics controller. The diagnostics controller should be able to supply the system with signals like MODE, SDI, DCLK, and the register clock (CLK). In order words, the diagnostics controller in itself is a supercontroller of the processing unit. It should also be noted that all sequential paths, except for the register files, should be converted to combinatorial paths if all the diagnostic parts are to break the sequential loops.

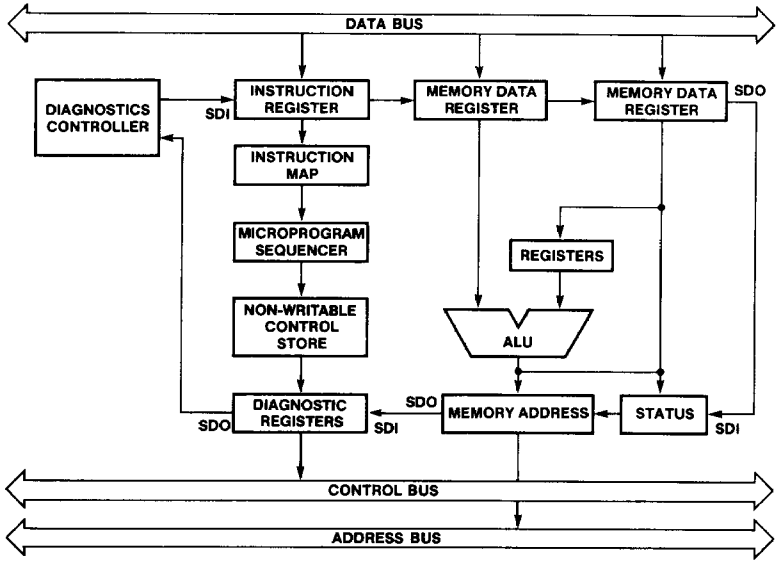

Figure 8. An application example of using diagnostic registers in a CPU using non-writable control store

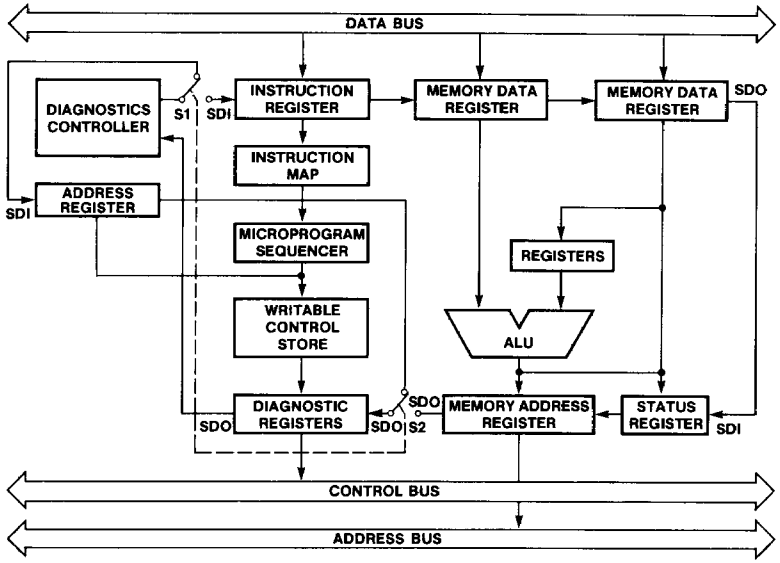

Figure 9. An application example of using diagnostic registers in a CPU using writable control store

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In normal operation, the diagnostic controller will make the diagnostic feature inactive by setting MODE = LOW and disabling DCLK and have the CLK free running.

When diagnostics are needed, the following sequence is performed:

1) Shift in diagnostic test data bit-by-bit. In order to perform this operation, CLK is disabled; MODE remains LOW; SDI contains the bit to be shifted in, and the diagnostic clock is enabled. This will continue until a full test vector is shifted into the shadow register.
2) MODE switches to HIGH. Then DCLK is disabled and CLK is enabled. The contents of the shadow register, which is the test vector, will be loaded into the output register.
3) The test result is set up at the inputs of the diagnostic registers. MODE switches to LOW again. DCLK is still disabled and CLK is still enabled. The test result will be clocked into the output register.
4) With MODE HIGH and DCLK enabled and CLK disabled, the test result will be clocked to the shadow register.
5) With MODE held LOW and DCLK still enabled and CLK still disabled, the test result can be shifted out and analyzed while another test vector is shifted in.

A block diagram of such a diagnostics controller is shown in Figure 10. The central control unit of this controller may be a disk-based unit or even a diagnostic PROM. Note that, in normal operation, MODE remains LOW and only CLK is active.

Figure 9 is an example with writable programmable control store where initialization of the control RAMs is necessary. This can be done by loading in a sequence of data and address through the diagnostics controller. What this controller must be able to do, in addition to what is described above (see Figure 10), is to disable the outputs from the microprogram sequencer and feed in the address through another diagnostic register. There is a switch, S1, which switches the SDI to the registers of the writable control store from some other register (in Figure 9, it is the memory address register) to the diagnostic 'control store address' register. The initialization data is shifted into the shadow register by resetting MODE to LOW and enabling DCLK. After all data is shifted into the shadow register, MODE and SDI are set HIGH and then followed by a CLK, a DCLK, and a write to control store. The CLK loads the present control store address in the output registers of the 'control store address' register, and the MODE = HIGH and SDI = HIGH will enable the inputs to the diagnostic register as outputs, so that the data in the shadow register can be written back to the control store.

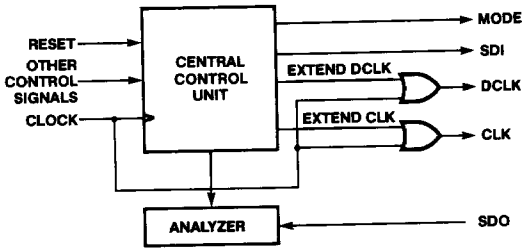

Figure 10. A diagnostic controller unit