MOTOROLA

Quad D-Type Flip-Flop With Common Clear and Common Clock

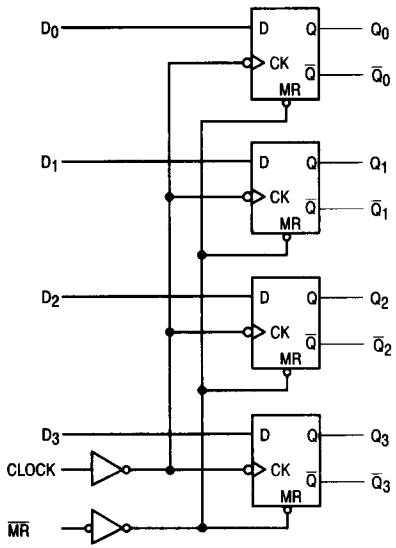
ELECTRICALLY TESTED PER:
MIL-M-38510/30107

The 54LS175 is a high-speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

The 'LS175 is fabricated with Schottky barrier diode process for high-speed and is completely compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset
- True and Complement Output
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC DIAGRAM



Please note that this logic diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Military 54LS175

MPO

AVAILABLE AS:

1) JAN: JM38510/30107BXA
2) SMD: N/A
3) 883: 54LS175/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{MR}$	1	1	2	GND
Q_0	2	2	3	OPEN
$\overline{Q}_0$	3	3	4	V_{CC}
D_0	4	4	5	V_{CC}
D_1	5	5	7	V_{CC}
$\overline{Q}_1$	6	6	8	V_{CC}
Q_1	7	7	9	OPEN
GND	8	8	10	GND
CK	9	9	12	V_{CC}
Q_2	10	10	13	OPEN
$\overline{Q}_2$	11	11	14	V_{CC}
D_2	12	12	15	V_{CC}
D_3	13	13	17	V_{CC}
$\overline{Q}_3$	14	14	18	V_{CC}
Q_3	15	15	19	OPEN
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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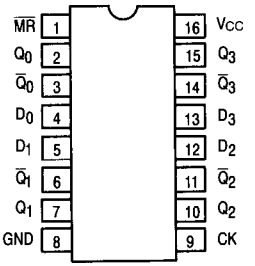
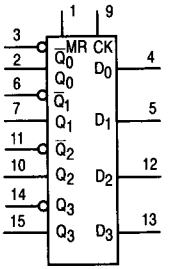
CONNECTION DIAGRAM



LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The 'LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH Clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow.

A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

	Inputs	Outputs	
	@ t_n	@ $t_n + 1$	
$\overline{MR}$	D	Q_n	$\overline{Q}_n$
H	L	L	H
H	H	H	L
L	X	L	H

t_n = Bit time before clock pulse
$t_n + 1$ = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

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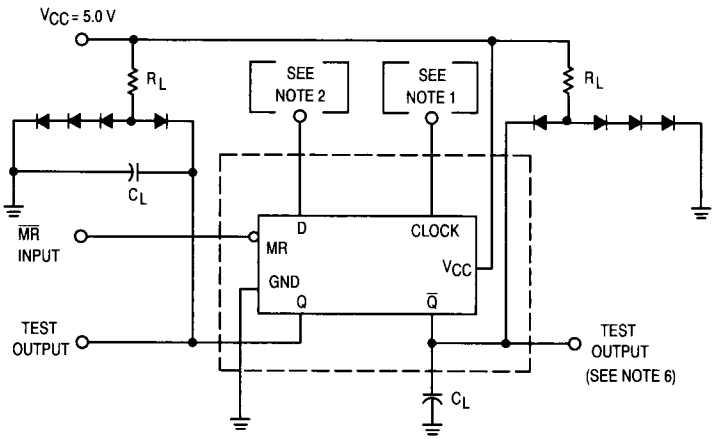
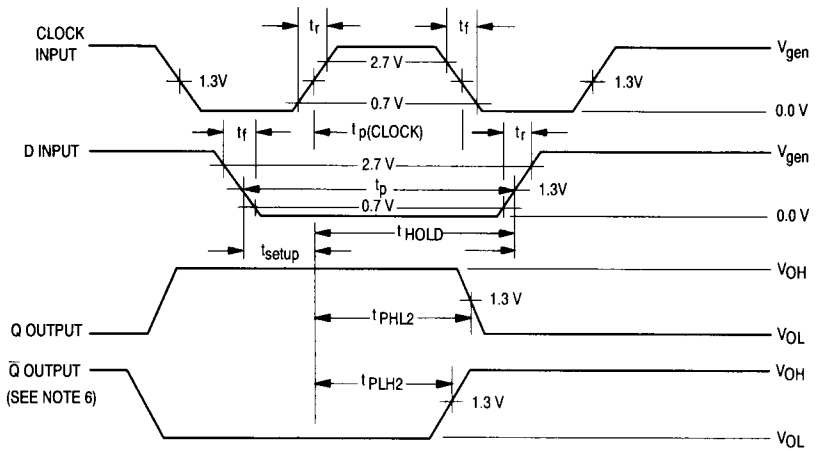
SYNCHRONOUS SWITCHING TEST CIRCUIT (LOW-LEVEL DATA)



WAVEFORMS



NOTES:

1. Clock input pulse has the following characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_{p(clock)}$ = 30 ns and PRR ≤ 1.0 MHz.
2. D input has the following characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, t_{setup} = 20 ns, t_{hold} = 5.0 ns, t_p = 25 ns and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. R_L = 2.0 kΩ ± 5.0%.
6. $\overline{Q}$ output applies to device type 07 only.

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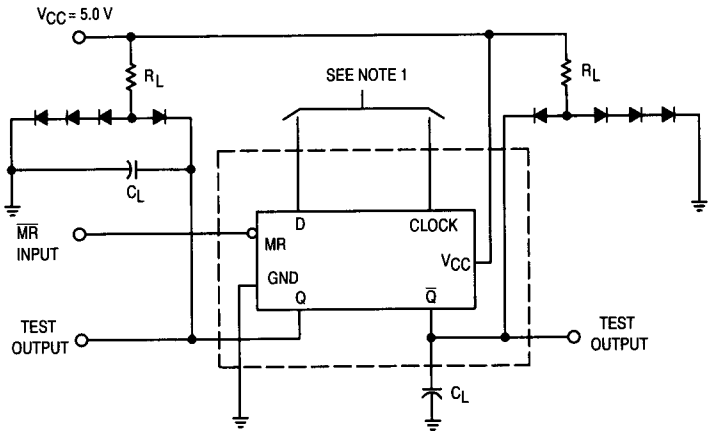
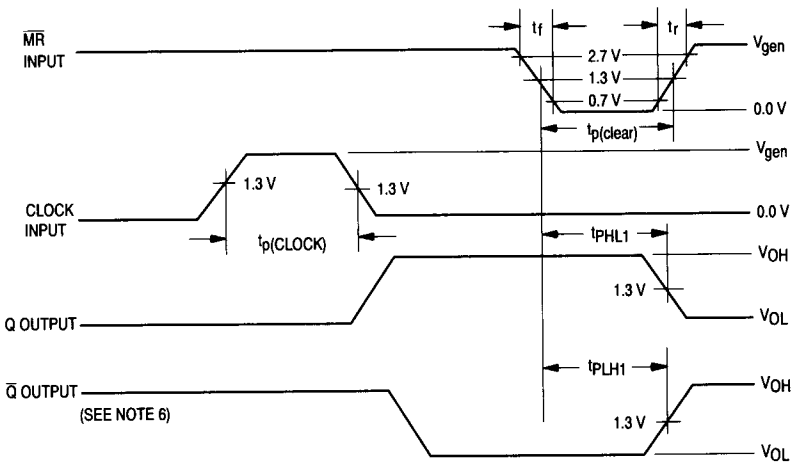
ASYNCHRONOUS SWITCHING TEST CIRCUIT



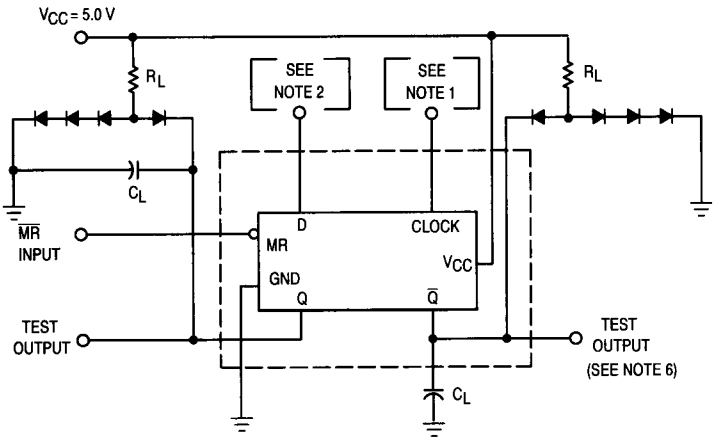
WAVEFORMS



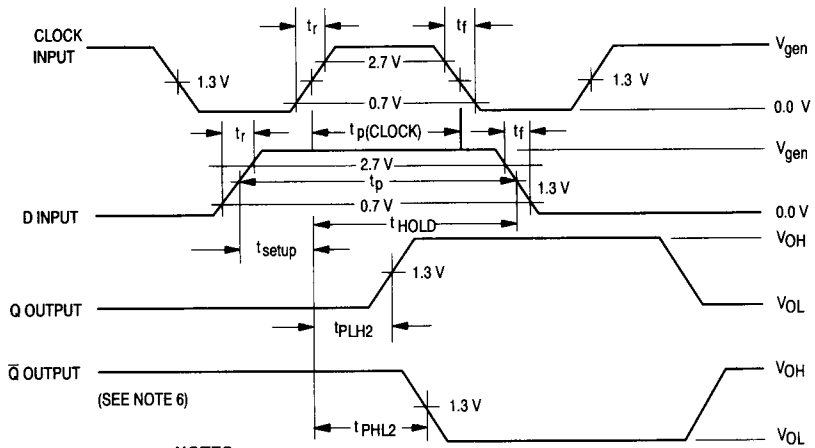
NOTES:

1. Clear input dominates regardless of the state of the clock or D inputs.
2. All diodes are 1N3064 or equivalent.
3. Clear input pulse characteristics:
   V_{gen} = 3.0 V, $t_f \leq 6.0$ ns, $t_r \leq 15$ ns, $t_{p(clear)}$ = 35 ns and PRR ≤ 1.0 MHz.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. R_L = 2.0 Ω ± 5.0 %.
6. $\overline{Q}$ output applies to device type 07 only.
7. Clock input pulse characteristics: $t_{p(clock)} \geq 25$ ns V_{gen} = 3.0 V and PRR ≤ 1.0 MHz.

SYNCHRONOUS SWITCHING TEST CIRCUIT (HIGH-LEVEL DATA)



WAVEFORMS



NOTES:

1. Clock input pulse has the following characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_{p(clock)}$ = 30 ns and PRR ≤ 1.0 MHz. When testing f_{MAX} PRR = (see table), $t_{p(clock)}$ = 20 ns $t_f = t_r = 6.0$ ns.
2. D input has the following characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, t_{setup} = 20 ns, t_{hold} = 5.0 ns, t_p = 25 ns and PRR is 50% of the clock PRR. For f_{MAX}, $t_f = t_r \leq 6.0$ ns.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. R_L = 2.0 kΩ ± 5.0%.
6. $\overline{Q}$ output applies to device type 07 only.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+125°C		− 55°C			
	Static Parameters	Subgroup 1		Subgroup 2		Subgourp 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA V_{IN} = 2.0 V or 0.7 V per truth table.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IN} = 2.0 V or 0.7 V per truth table.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} =4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{HH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current (D)	− 0.16	− 0.4	− 0.16	− 0.4	− 0.16	− 0.4	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs are open.
I_L	Logical "0" Input Current ($\overline{MR}$)	− 0.105	− 0.38	− 0.105	− 0.38	− 0.105	− 0.38	mA	V_{CC} = 4.5 V, other inputs are open. $\overline{MR}$ = 0.4 V
	(CK)	− 0.16	− 0.4	− 0.16	− 0.4	− 0.16	− 0.4		CK = 0.4 V
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN}(D) = 4.5 V, $\overline{MR}$ = 4.5 V, other data inputs are open.
I_{CC}	Power Supply Current		18		18		18	mA	V_{CC}= 5.5 V, V_{IN} = 5.5 V, $\overline{MR}$ = 5.5 V. other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC}= 4.5 V
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC}= 4.5 V
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Clear to Output	5.0 —	45 30	5.0 —	55 50	5.0 —	55 50	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Clear to Output	5.0 —	32 30	5.0 —	51 46	5.0 —	51 46	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output Clock to Output	5.0 —	40 25	5.0 —	55 50	5.0 —	56 50	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Clock to Output	5.0 —	35 25	5.0 —	46 41	5.0 —	46 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25		25		25		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.

NOTES:

1. Voltage measurements are to be made with respect to network ground terminal.
2. R_L = 2.0 kΩ ± 5.0%.
3. f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be 1/2 the input frequency.
4. Clock and Reset inputs need to be in the proper configuration for specified output conditions.
5. The limits specified for C_L = 15 pF are guaranteed, but not tested.
6. Tests shall be performed in sequence, attributes data only.

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