- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs**

SN54ABT843 . . . JT OR W PACKAGE
SN74ABT843 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)

```
        _____
OE  [ 1      24 ]  VCC
1D  [ 2      23 ]  1Q
2D  [ 3      22 ]  2Q
3D  [ 4      21 ]  3Q
4D  [ 5      20 ]  4Q
5D  [ 6      19 ]  5Q
6D  [ 7      18 ]  6Q
7D  [ 8      17 ]  7Q
8D  [ 9      16 ]  8Q
9D  [ 10     15 ]  9Q
CLR [ 11     14 ]  PRE
GND [ 12     13 ]  LE
```

SN54ABT843 . . . FK PACKAGE
(TOP VIEW)

```
          2D 1D OE NC VCC 1Q 2Q
           4  3  2  1  28 27 26
3D  [ 5                  25 ]  3Q
4D  [ 6                  24 ]  4Q
5D  [ 7                  23 ]  5Q
NC  [ 8                  22 ]  NC
6D  [ 9                  21 ]  6Q
7D  [ 10                 20 ]  7Q
8D  [ 11                 19 ]  8Q
           12 13 14 15 16 17 18
          9D CLR GND NC LE PRE 9Q
```

NC – No internal connection

description

The 'ABT843 9-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

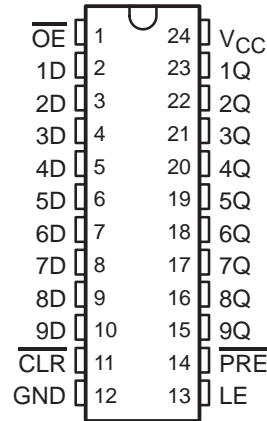The nine transparent D-type latches provide true data at the outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.
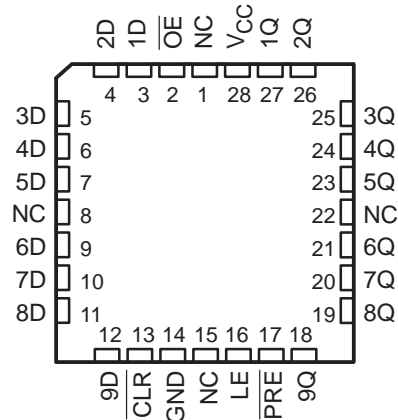
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT843 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT843 is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

FUNCTION TABLE

INPUTS					OUTPUT
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	$\overline{\text{OE}}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

logic symbol[†]

$\overline{\text{OE}}$	1	▷ EN		
$\overline{\text{PRE}}$	14	▷ S2		
$\overline{\text{CLR}}$	11	▷ R		
LE	13	C1		

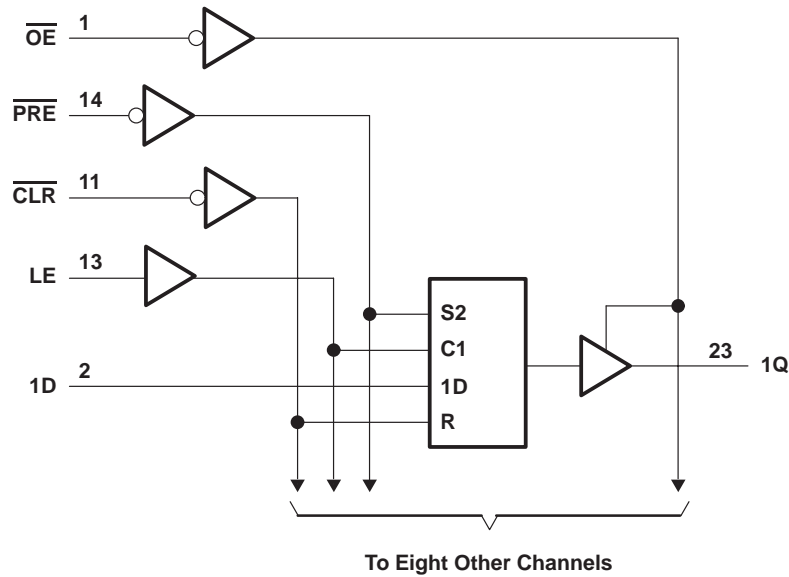| 1D | 2 | 1D | 2 ▽ | 23 | 1Q |
2D	3			22	2Q
3D	4			21	3Q
4D	5			20	4Q
5D	6			19	5Q
6D	7			18	6Q
7D	8			17	7Q
8D	9			16	8Q
9D	10			15	9Q
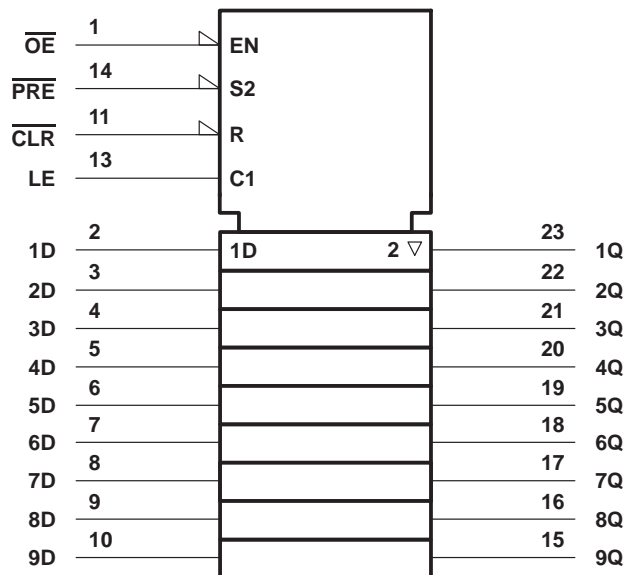
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, and W packages.

TEXAS INSTRUMENTS

logic diagram (positive logic)

To Eight Other Channels

Pin numbers shown are for the DB, DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range , V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT843 .... 96 mA
SN74ABT843 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 104°C/W
DW package .... 81°C/W
NT package .... 67°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT843 MIN	SN54ABT843 MAX	SN74ABT843 MIN	SN74ABT843 MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3:   Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25°C$ MIN	$T_A = 25°C$ TYP†	$T_A = 25°C$ MAX	SN54ABT843 MIN	SN54ABT843 MAX	SN74ABT843 MIN	SN74ABT843 MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
	V_{CC} = 4.5 V	I_{OH} = −24 mA				2				
		I_{OH} = −32 mA	2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA					0.55			V
		I_{OL} = 64 mA			0.55*				0.55	
V_{hys}				100						mV
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	μA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	μA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V			−10		−10		−10	μA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	μA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	μA
I_O§	V_{CC} = 5.5 V, V_O = 2.5 V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = Open, V_I = V_{CC} or GND	Outputs high		1	250		250		250	μA
		Outputs low		24	34		34		34	mA
		Outputs disabled		0.5	250		250		250	μA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			4						pF
C_o	V_O = 2.5 V or 0.5 V			7						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TEXAS
INSTRUMENTS

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

				V_{CC} = 5 V, T_A = 25°C		SN54ABT843		SN74ABT843		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low		5.5		5.5		5.5		ns
		$\overline{PRE}$ low		4.5		4.5		4.5		
		LE low		3.3		3.3		3.4		
t_{su}	Setup time	Data before LE↓	Low	2.5		2.5		2.5		ns
			High	3		3		3		
		$\overline{PRE}$ inactive		1.6		1.6		1.6		
		$\overline{CLR}$ inactive		2		2		2		
t_h	Hold time, data after LE↓	High		1		1		1		ns
		Low		1.5[†]		2.3[†]		1.5[†]		

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT843		SN74ABT843		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.2[†]	3.8	5.2	1.2[†]	7.8	1.2[†]	6.7[†]	ns
t_{PHL}			1.5[†]	3.4	6.3	1.5[†]	7.3	1.5[†]	7.2	
t_{PLH}	LE	Q	1.7[†]	4.4	5.6	1.7[†]	8.3	1.7[†]	7.2[†]	ns
t_{PHL}			1.9[†]	4.1	6.3	1.3[†]	7.2	1.9[†]	6.9	
t_{PLH}	$\overline{PRE}$	Q	2.2	5	6.2	2.2	8.3	2.2	7.4	ns
t_{PHL}			2.1[†]	4.1	6.5	2.1[†]	7.5	2.1[†]	7.2	
t_{PLH}	$\overline{CLR}$	Q	2[†]	4.4	6.3	2[†]	7.6	2[†]	7.1	ns
t_{PHL}			1.9[†]	4.5	6.8	1.9[†]	8.1	1.9[†]	8	
t_{PZH}	$\overline{OE}$	Q	1	3.4	4.5[†]	1	6.4	1	5.7[†]	ns
t_{PZL}			2	4.3	5.7[†]	2	6.6	2	6.5	
t_{PHZ}	$\overline{OE}$	Q	2.4[†]	4.9	6.2	2.4[†]	7.3	2.4[†]	6.8	ns
t_{PLZ}			1.5[†]	4.2	6.3	1.5[†]	7	1.5[†]	5.9[†]	

† This data sheet limit may vary among suppliers.
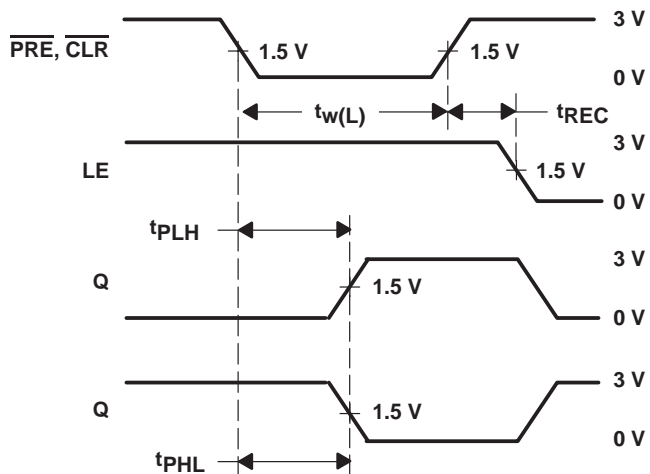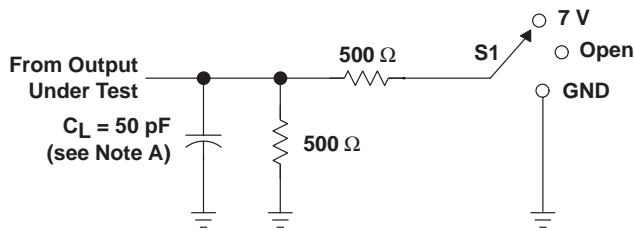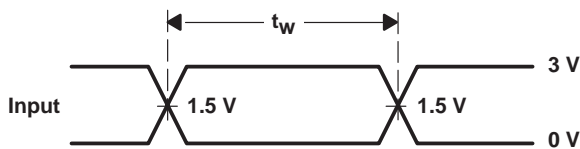
recovery-time waveform

Figure 1. $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ Pulse Duration, $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ to Output Delay,
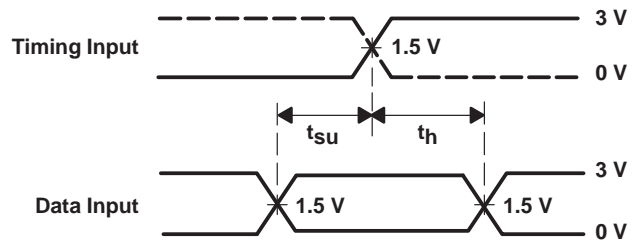and $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ to Latch-Enable Recovery Time

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

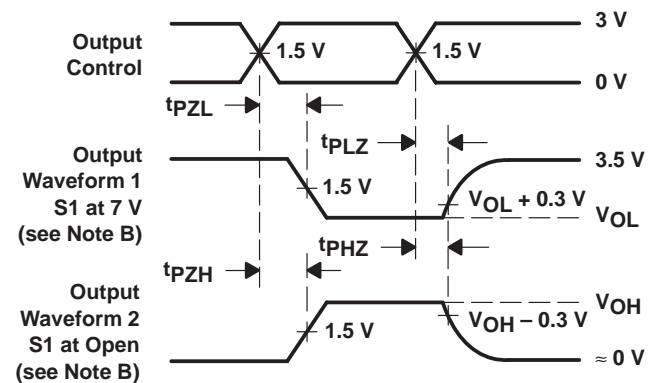| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
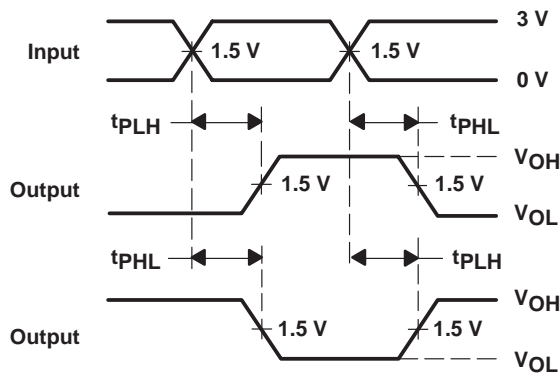
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG | APPLICATION NOTES | USER GUIDES | MORE LITERATURE

PRODUCT SUPPORT: TRAINING

SN54ABT843, 9-Bit Bus-Interface D-type Latches With 3-State Outputs
DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ABT843	SN74ABT843
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-32/64
No. of Outputs	9	9
Static Current		17.12
th (ns)		1.5
tpd max (ns)		7.2
tsu (ns)		3.0
Logic	True	True

FEATURES   ▲Back to Top

- State-of-the-Art **EPIC**-II **B**^{TM} BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
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EPIC-IIB is a trademark of Texas Instruments Incorporated.

DESCRIPTION   ▲Back to Top

The 'ABT843 9-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine transparent D-type latches provide true data at the outputs.

A buffered output-enable (OE\) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE\ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT843 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT843 is characterized for operation from -40°C to 85°C.

Product Folder: SN54ABT843, 9-Bit Bus-Interface D-type Latches With 3-State Outputs

TECHNICAL DOCUMENTS

To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Full datasheet in Acrobat PDF: sn54abt843.pdf (120 KB, Rev.D) (Updated: 05/01/1997)

APPLICATION NOTES

View Application Notes for Digital Logic

- Advanced BiCMOS Technology (ABT) Logic Characterization Information (Rev. B) (SCBA008B - Updated: 06/01/1997)
- Advanced BiCMOS Technology (ABT) Logic Enables Optimal System Design (Rev. A) (SCBA001A - Updated: 03/01/1997)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices (Rev. A) (SCBA006A - Updated: 12/01/1996)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 - Updated: 05/10/2002)
- Quad Flatpack No-Lead Logic Packages (Rev. C) (SCBA017C - Updated: 11/22/2002)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG

DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 09:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 09:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (ºC)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME	DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
5962-9571201Q3A	ACTIVE	LCCC (FK) | 28	-55 TO 125		View Contents	1KU | 15.99	1	0*	3770 | 20 May	8 WKS	None Reported View Distributors		
									>10k | 27 May				
5962-9571201QKA	ACTIVE	CFP (W) | 24	-55 TO 125		View Contents	1KU | 13.20	1	0*	>10k | 20 May	8 WKS	None Reported View Distributors		
5962-9571201QLA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 9.65	1	0*	>10k | 20 May	8 WKS	None Reported View Distributors		

Product Folder: SN54ABT843, 9-Bit Bus-Interface D-type Latches With 3-State Outputs

SNJ54ABT843FK	ACTIVE	LCCC (FK)	| 28	-55 TO 125	5962-9571201Q3A	View Contents	1KU | 15.99	1	0*	3889 | 20 May	8 WKS	None Reported View Distributors	
										>10k | 27 May			
SNJ54ABT843JT	ACTIVE	CDIP (JT)	| 24	-55 TO 125	5962-9571201QLA	View Contents	1KU | 9.65	1	435*	>10k | 20 May	8 WKS	None Reported View Distributors	
SNJ54ABT843W	ACTIVE	CFP (W)	| 24	-55 TO 125	5962-9571201QKA	View Contents	1KU | 12.97	1	0*	>10k | 20 May	8 WKS	None Reported View Distributors	

Table Data Updated on: 4/17/2003