HARRIS SEMICONDUCTOR

CD74FCT646T, CD74FCT648T, CD74FCT651T, CD74FCT652T, CD74FCT2646T, CD74FCT2652T

December 1996

Fast CMOS Octal Registered Transceivers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed, Lower Power Consumption**
- **25Ω Series Resistor on All Outputs (FCT2XXX Only)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

These devices are designed with a bus transceiver with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The CD74FCT651T, CD74FCT652T and CD74FCT2652T utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The CD74FCT646T, CD74FCT2646T and CD74FCT648T utilize the enable control ($\overline{G}$) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74FCT646T is a non-inverting option of the CD74FCT648T. The CD74FCT652T is a non-inverting option of the CD74FCT651T.

The CD74FCT2646T and CD74FCT2652T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT646ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT646ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT646CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT646CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT646DTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT646DTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT646TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT646TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT648ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT648ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT648CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT648CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT648TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT648TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT651ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT651ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT651CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT651CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT651TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT651TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT652ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT652ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT652CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT652CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT652DTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT652DTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT652TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT652TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2646ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2646ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2646TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2646TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2652ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2652ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2652CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2652CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2652TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2652TQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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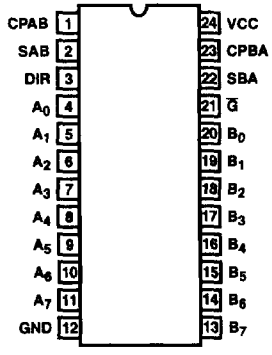
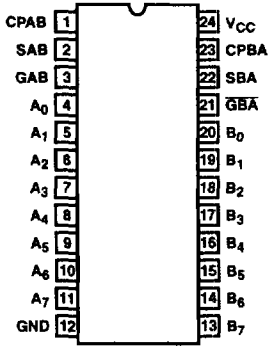
Pinouts

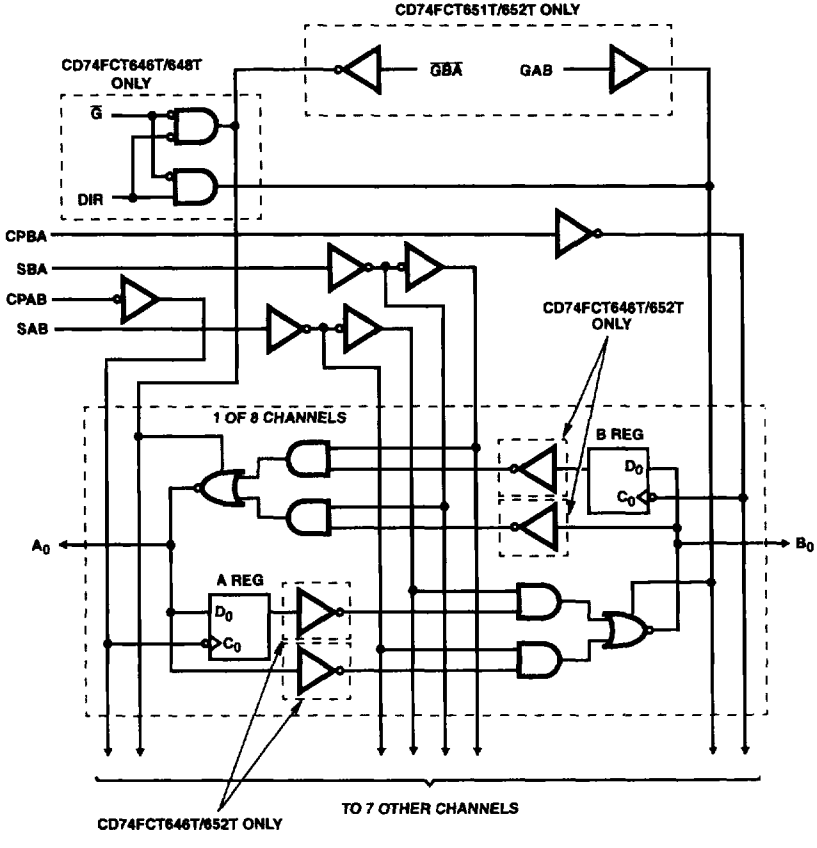
CD74FCT646T, CD74FCT648T, CD74FCT2646T
(QSOP, SOIC)
TOP VIEW



CD74FCT651T, CD74FCT652T, CD74FCT2652T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



CD74FCT646T, CD74FCT2646T, CD74FCT648T TRUTH TABLE

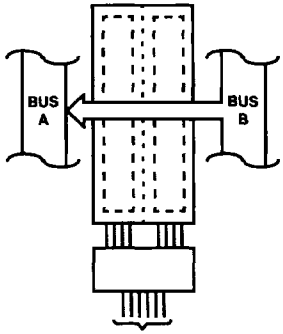
CD74FCT646T, CD74FCT2646T	CD74FCT648T	INPUTS						(NOTE 2) DATA I/O	
FUNCTION/OPERATION	FUNCTION/OPERATION	$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7
Isolation	Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	Store A and B Data	H	X	↑	↑	X	X	Input	Input
Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus	L	L	X	H or L	X	H	Output	Input
Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus	L	H	H or L	X	H	X	Input	Output

CD74FCT651T, CD74FCT652T, CD74FCT2652T TRUTH TABLE

CD74FCT651T	CD74FCT652T, CD74FCT2652T	INPUTS						(NOTE 2) DATA I/O	
FUNCTION/OPERATION	FUNCTION/OPERATION	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7
Isolation	Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	Store A and B Data	L	H	↑	↑	X	X	Input	Input
Store A, Hold B	Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified (Note 1)
Store A in Both Registers (Note 3)	Store A in Both Registers	H	H	↑	↑	X (Note 2)	X	Input	Output
Hold A, Store B	Hold A, Store B	L	X	H or L	↑	X	X	Unspecified (Note 1)	Input
Store B in Both Registers (Note 4)	Store B in Both Registers	L	L	↑	↑	X	X (Note 2)	Output	Input
Real Time $\overline{B}$ Data to A Bus	Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus	L	L	X	H or L	X	H	Output	Input
Real Time $\overline{A}$ Data to B Bus	Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus	H	H	H or L	X	H	X	Input	Output
Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

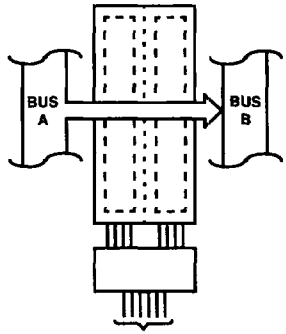
NOTES:

1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.



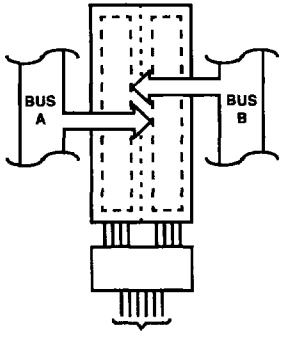
646T/648T/2646T	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
651T/652T/2652T	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

FIGURE 1. REAL-TIME TRANSFER BUS B TO A



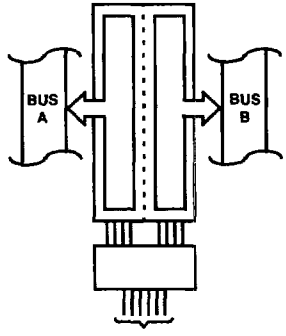
646T/648T/2646T	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X
651T/652T/2652T	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X

FIGURE 2. REAL-TIME TRANSFER BUS A TO B



646T/648T/2646T	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X
651T/652T/2652T	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X

FIGURE 3. STORAGE FROM A AND/OR B



646T/648T/2646T (NOTE 5)	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X
651T/652T/2652T	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or L	H or L	H	H

FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

NOTE:

5. The CD74FCT646T and CD74FCT2646T cannot transfer data to A bus and B bus simultaneously.

Pin Descriptions

PIN NAME	DESCRIPTION
A_0-A_7	Data Register A Inputs Data Register B Outputs
B_0-B_7	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (CD74FCT646T, CD74FCT648T, CD74FCT2646T)
GAB, $\overline{GBA}$	Output Enable Inputs (CD74FCT651T, CD74FCT652T, CD74FCT2652T)
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

6. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 7) TEST CONDITIONS		MIN	(NOTE 8) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.55	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.55	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}, I_{OZL}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
			V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 9), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 11)	-	0.5	2	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 7) TEST CONDITIONS		MIN	(NOTE 8) TYP	MAX	UNITS
Supply Current per Input per MHz (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{G}$ or DIR = GND or GAB = $\overline{GBA}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND f_i = 5MHz One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 13)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND f_i = 2.5MHz, 50% Duty Cycle Eight Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.8	7.3	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	T (NOTE 16) MIN	T MAX	AT (NOTE 16) MIN	AT MAX	(NOTE 18) CT (NOTE 16) MIN	CT MAX	(NOTE 18, 19) DT (NOTE 16) MIN	DT MAX	UNIT
CD74FCT646T, CD74FCT2646T, CD74FCT648T											
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	1.5	4.8	ns
Output Enable Time $\overline{G}$, DIR to Bus	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	2.0	14.0	2.0	9.8	1.5	7.8	1.5	7.3	ns
Output Disable Time $\overline{G}$, DIR to Bus (Note 17)	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
Propagation Delay SBA or SAB to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	1.5	-	ns
Clock Pulse Width HIGH or LOW (Note 17)	t_W	C_L = 50pF R_L = 500Ω	6.0	-	5.0	-	5.0	-	5.0	-	ns
CD74FCT651T, CD74FCT652T, CD74FCT2652T											
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
Output Enable Time $\overline{GBA}$, GAB to Bus	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	2.0	12.5	2.0	9.8	1.5	7.8	1.5	7.3	ns

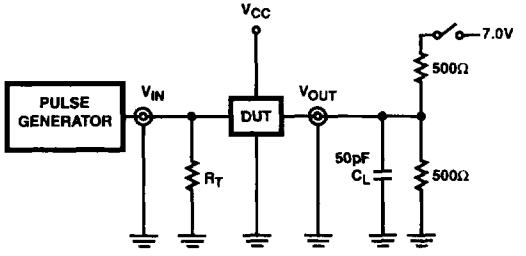
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	T (NOTE 16) MIN	T MAX	AT (NOTE 16) MIN	AT MAX	(NOTE 18) CT (NOTE 16) MIN	CT MAX	(NOTE 18, 19) DT (NOTE 16) MIN	DT MAX	UNIT
Output Disable Time $\overline{GBA}$, GAB to Bus (Note 17)	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.0	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
Propagation Delay SBA or SAB to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	1.5	-	ns
Clock Pulse Width HIGH or LOW (Note 17)	t_W	C_L = 50pF R_L = 500Ω	6.0	-	5.0	-	5.0	-	5.0	-	ns

NOTES:

7. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
8. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
9. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Not applicable to CD74FCT2646T, CD74FCT2652T.
19. Not applicable to CD74FCT648T.
20. Not applicable to CD74FCT651T or CD74FCT652T.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:
C_L = Load capacitance, includes jig and probe capacitance.
R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

21. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

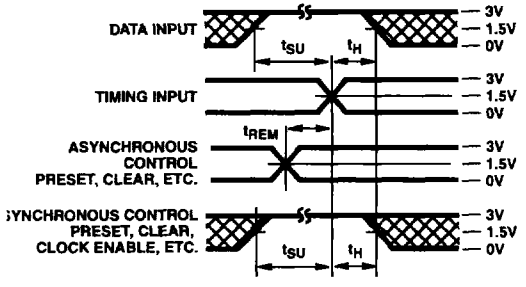


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

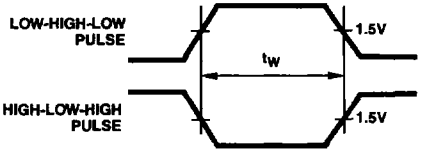


FIGURE 7. PULSE WIDTH

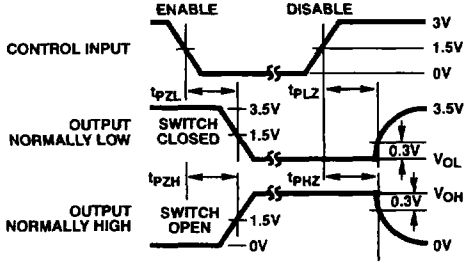


FIGURE 8. ENABLE AND DISABLE TIMING

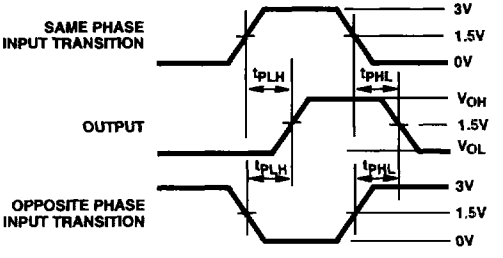


FIGURE 9. PROPAGATION DELAY

4 OCTAL 5V FCT 5V FCT 25Ω